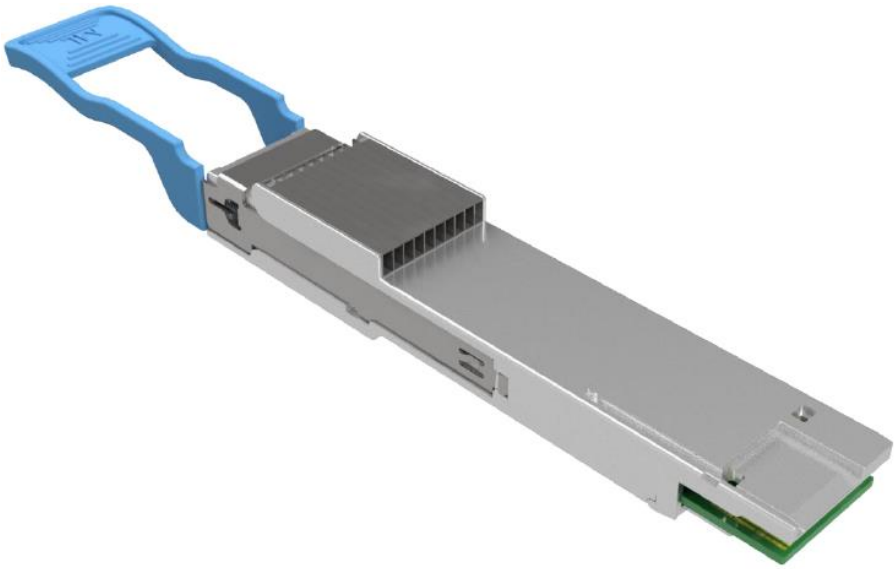
ML4062-ALB1-2A/B-112

Technical Reference

QSFP-DD Electrical Active Loopback Module
CMIS 5.0 Compliant



Innovation for the next generation

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1 Overview

The **ML4062-ALB1-2A/B-112** is an active electrical loopback that provides a straightforward method to test QSFP-DD ports at every level of the switch production process. The active electrical loopback (ALB) acts as a fully-featured QSFP-DD transceiver and is used for testing QSFP-DD transceiver ports under board level tests.
The active electrical loopback includes a transceiver chip, where 8xTX channels and 8xRX channels are available. Data is transmitted from the host to the TX input port of the active loopback, and retimed signal is received by the host via the RX output port of the active loopback.
The **ML4062-ALB1-2A/B-112** is ideal for R&D validation, production testing, and field testing. The **ML4062-ALB1-2A/B-112** follows the **CMIS Rev 5.0** standard and is packaged in standard MSA housing compatible with all QSFP-DD power classes.

1.1 ML4062-ALB1-2A/B-112 QSFP-DD active loopback | Key Features

- QSFP-DD MSA Form Factor
- MSA Compatible Configuration and EEPROM
- Programmable MSA memory pages
- Custom memory maps
- I2C Interface
- USB Interface
- Electrical transceiver chip
- Separate daughter card for power spots
- Additional programmable power heaters, dissipating up to 19W
- Two temperature sensors
- Voltage sensor
- Cut-off temperature preventing module overheating

1.2 Recommended Operating Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		-40		85	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.6	V
Input/output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω

1.3 Ordering Information

The module can be ordered with one of the two available heatsink designs, as shown in the table below.

Option	Part Number	Description
#1 – Type 2A	ML4062-ALB1-2A-112	Type 2A heatsink
#2 – Type 2B	ML4062-ALB1-2B-112	Type 2B heatsink

2 Management Data Interface – I2C

The **ML4062-ALB1-2A/B-112** supports the I2C interface.

2.1 I2C Signals, Addressing and Frame Structure

2.1.1 I2C Frame

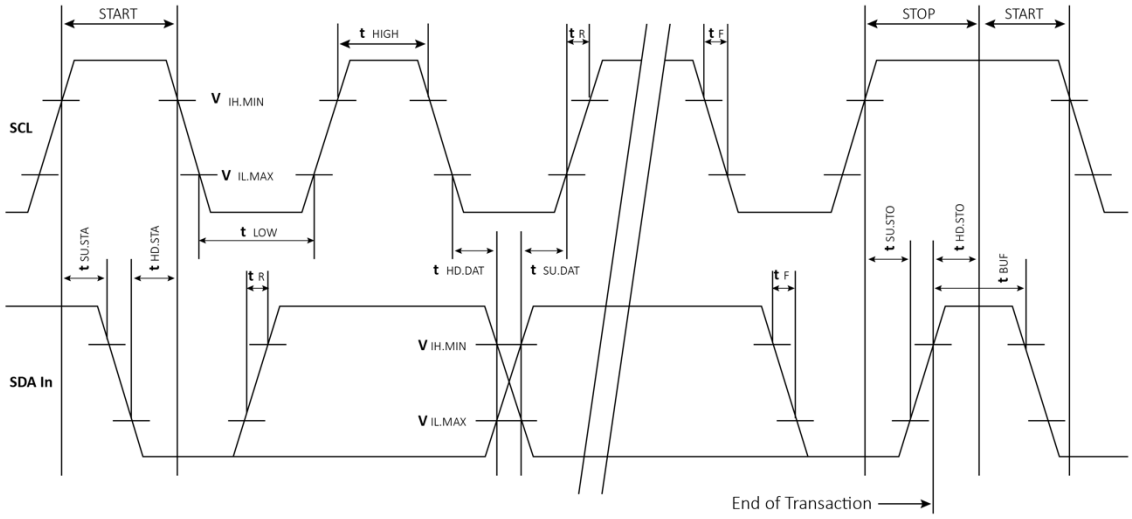

Figure 1: QSFP-DD Timing Diagram

Before initiating a 2-wire serial bus communication, provide setup time on the ModSelL line of all modules on the 2-wire bus. Do not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied. The 2-wire serial interface address of the QSFP-DD module is 1010000X (A0h).

In order to allow access to multiple QSFP-DD modules on the same 2-wire serial bus, the QSFP-DD pinout includes a ModSelL or module select pin. This pin (which is pulled high or deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module does not respond to or accept 2-wire serial bus instructions unless it is selected.

2.1.2 Management Timing Parameters

The timing parameters for the 2-Wire interface to the QSFP-DD module are shown in the table below:

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}	10	1015	kHz
Clock Pulse Width Low	t_{LOW}	0.35		us
Clock Pulse Width High	t_{High}	0.35		us
Time bus free before new transmission can start	t_{BUF}	1.5		us
START Hold Time	$t_{HD.STA}$	0.08		us
START Set-up Time	$t_{SU.STA}$	0.4		us
Data In Hold Time	$t_{HD.DAT}$	0.1		us
Data in Set-up Time	$t_{SU.DAT}$	0.1		us
STOP Set-up Time	$t_{SU.STO}$	0.4		us

2.1.3 Memory Specifications

QSFP-DD memory transaction timings are given in the above table.

Parameter	Symbol	Min	Max	Unit
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		125	us
Complete Single Write	tWR		40	ms

2.1.4 Device Addressing and Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the QSFP-DD in 8-bit words. Every Byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.
STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one-bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word.

Memory (Management Interface) Reset: After an interruption in protocol, power loss, or system reset, the QSFP-DD Module management interface can be reset. Memory reset only resets the QSFP-DD transceiver management interface (to correct a hung bus) leaving all other module functionality intact.

Device Addressing: QSFP-DD devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 2. This is common to all QSFP-DD devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 2: QSFP-DD Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address (with ModSelL in the low state) the QSFP-DD Module will output a zero (ACK) on the SDA line to acknowledge the address.

2.2 QSFP-DD Memory Map

2.2.1 Full Map

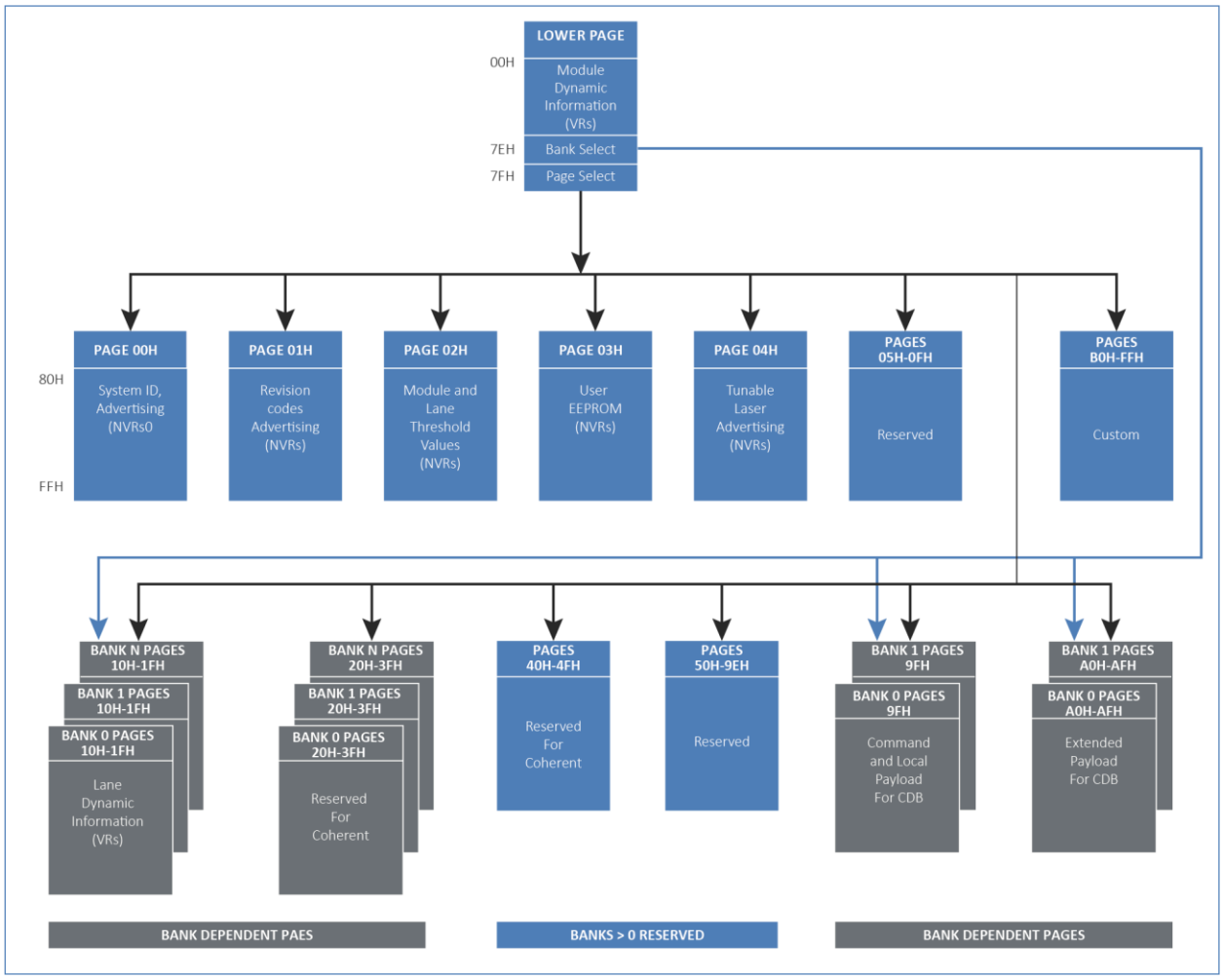

Figure 3: QSFP-DD Memory Map

This section defines the Memory Map for QSFP-DD transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP-DD devices. The structure of the memory is shown in Figure 3. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed.

2.2.2 ML4062-ALB1-2A/B-112 Memory Map

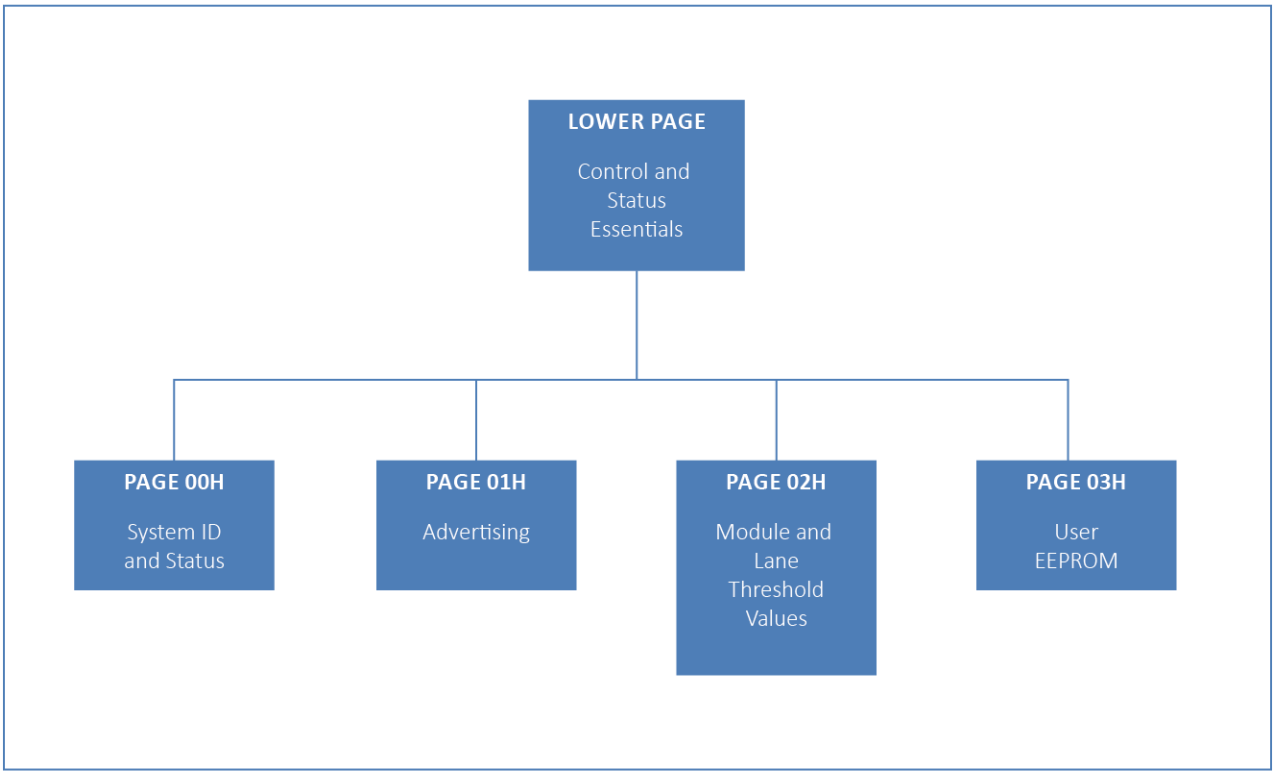

Figure 4: Implemented Memory Map

2.2.3 Memory Content

The table below shows the memory content.

Address	Hex	Dec	ASCII	MSA Description
LowMem 0(00h)	0x18	24		Identifier
LowMem 1(01h)	0x50	80	P	Revision Compliance
LowMem 2(02h)	0x04	4		Flat-mem / TWI Max Speed
LowMem 3(03h)	0x00	0		Module State / Software interrupt
LowMem 4(04h)	0x00	0		Bank 0 flag summary
LowMem 5(05h)	0x00	0		Bank 1 flag summary
LowMem 6(06h)	0x00	0		Bank 2 flag summary
LowMem 7(07h)	0x00	0		Bank 3 flag summary
LowMem 8(08h)	0x00	0		Data Path/Module FW fault and Module State changed flag
LowMem 9(09h)	0x00	0		Latched VCC3.3/Temp Alarm and Warning
LowMem 10(0Ah)	0x00	0		Latched AUX1/2 Alarm and Warning

LowMem 11(0Bh)	0x00	0		Latched Vendor Defined/AUX3 Alarm and Warning
LowMem 12(0Ch)	0x00	0		Reserved
LowMem 13(0Dh)	0x00	0		Custom
LowMem 14(0Eh)				Internally measured Temperature T.S.2 MSB
LowMem 15(0Fh)				Internally measured Temperature T.S.2 LSB
LowMem 16(10h)				Internally measured Supply 3.3v MSB
LowMem 17(11h)				Internally measured Supply 3.3v LSB
LowMem 18-23 (12h-17h)	0x00	0		
LowMem 24(18h)				Internally Measured Retimer Chip Temperature MSB
LowMem 25(19h)				Internally Measured Retimer ChipTemperature LSB
LowMem 26(1Ah)	0x40	64	@	Software reset / Low power control
LowMem 27-38 (1Bh-26h)	0x00	0		
LowMem 39(27h)	0x01	1		Major FW Rev
LowMem 40(28h)	0x02	2		Minor FW Rev
LowMem 41-84 (29h-54h)	0x00	0		
LowMem 85(55h)	0x04			Media Type
LowMem 86(56h)	0x51			Host Interface ID AppSel code 1
LowMem 87(57h)	0xBF			Media Interface ID AppSel code 1
LowMem 88(58h)	0x88			Host and Media Lane Count AppSel code 1
LowMem 89(59h)	0x01			Host Lane Assignment Options AppSel code 1
LowMem 90(5Ah)	0x4F			Host Interface ID AppSel code 2
LowMem 91(5Bh)	0xBF			Media Interface ID AppSel code 2
LowMem 92(5Ch)	0x44			Host and Media Lane Count AppSel code 2
LowMem 93(5Dh)	0x11			Host Lane Assignment Options AppSel code 2
LowMem 94(5Eh)	0x11			Host Interface ID AppSel code 3
LowMem 95(5Fh)	0xBF			Media Interface ID AppSel code 3
LowMem 96(60h)	0x88			Host and Media Lane Count AppSel code 3
LowMem 97(61h)	0x01			Host Lane Assignment Options AppSel code 3
LowMem 98(62h)	0x0E			Host Interface ID AppSel code 4
LowMem 99(63h)	0xBF			Media Interface ID AppSel code 4

LowMem 100(64h)	0x88			Host and Media Lane Count AppSel code 4
LowMem 101(65h)	0x01			Host Lane Assignment Options AppSel code 4
LowMem 102(66h)	0x52			Host Interface ID AppSel code 5
LowMem 103(67h)	0xBF			Media Interface ID AppSel code 5
LowMem 104(68h)	0x88			Host and Media Lane Count AppSel code 5
LowMem 105(69h)	0x01			Host Lane Assignment Options AppSel code 5
LowMem 106(6Ah)	0x50			Host Interface ID AppSel code 6
LowMem 107(6Bh)	0xBF			Media Interface ID AppSel code 6
LowMem 108(6Ch)	0x44			Host and Media Lane Count AppSel code 6
LowMem 109(6Dh)	0x11			Host Lane Assignment Options AppSel code 6
LowMem 110(6Eh)	0x0A			Host Interface ID AppSel code 7
LowMem 111(6Fh)	0xBF			Media Interface ID AppSel code 7
LowMem 112(70h)	0x11			Host and Media Lane Count AppSel code 7
LowMem 113(71h)	0xFF			Host Lane Assignment Options AppSel code 7
LowMem 114(72h)	0x05			Host Interface ID AppSel code 8
LowMem 115(73h)	0xBF			Media Interface ID AppSel code 8
LowMem 116(74h)	0x11			Host and Media Lane Count AppSel code 8
LowMem 117(75h)	0xFF			Host Lane Assignment Options AppSel code 8
LowMem 118-125(76h-7D)	0x00			
LowMem 126(7Eh)	0x00	0		Bank Select Byte
LowMem 127(7Fh)	0x00	0		Page Select Byte
Page00 128(80h)	0x18	24		Identifier
Page00 129(81h)	0x4D	77	M	Vendor Name
Page00 130(82h)	0x55	85	U	Vendor Name
Page00 131(83h)	0x4C	76	L	Vendor Name
Page00 132(84h)	0x54	84	T	Vendor Name
Page00 133(85h)	0x49	73	I	Vendor Name
Page00 134(86h)	0x4C	76	L	Vendor Name
Page00 135(87h)	0x41	65	A	Vendor Name
Page00 136(88h)	0x4E	78	N	Vendor Name

Page00 137(89h)	0x45	69	E	Vendor Name
Page00 138(8Ah)	0x20	32		Vendor Name
Page00 139(8Bh)	0x20	32		Vendor Name
Page00 140(8Ch)	0x20	32		Vendor Name
Page00 141(8Dh)	0x20	32		Vendor Name
Page00 142(8Eh)	0x20	32		Vendor Name
Page00 143(8Fh)	0x20	32		Vendor Name
Page00 144(90h)	0x20	32		Vendor Name
Page00 145(91h)	0x00	0		Vendor OUI
Page00 146(92h)	0x00	0		Vendor OUI
Page00 147(93h)	0x00	0		Vendor OUI
Page00 148(94h)	0x34	52	4	Vendor PN
Page00 149(95h)	0x30	48	0	Vendor PN
Page00 150(96h)	0x36	54	6	Vendor PN
Page00 151(97h)	0x32	50	2	Vendor PN
Page00 152(98h)	0x41	65	A	Vendor PN
Page00 153(99h)	0x4C	76	L	Vendor PN
Page00 154(9Ah)	0x42	66	B	Vendor PN
Page00 155(9Bh)	0x31	49	1	Vendor PN
Page00 156(9Ch)	0x32	50	2	Vendor PN
Page00 157(9Dh)	0x42	66	B	Vendor PN
Page00 158(9Eh)	0x31	49	1	Vendor PN
Page00 159(9Fh)	0x31	49	1	Vendor PN
Page00 160(A0h)	0x32	50	2	Vendor PN
Page00 161(A1h)	0x2E	46	.	Vendor PN
Page00 162(A2h)	0x33	51	3	Vendor PN
Page00 163(A3h)	0x30	48	0	Vendor PN
Page00 164(A4h)	0x31	49	1	Vendor Rev
Page00 165(A5h)	0x30	48	0	Vendor Rev
Page00 166(A6h)	0x20	32		Vendor SN

Page00 167(A7h)	0x20	32		Vendor SN
Page00 168(A8h)	0x20	32		Vendor SN
Page00 169(A9h)	0x20	32		Vendor SN
Page00 170(AAh)	0x20	32		Vendor SN
Page00 171(ABh)	0x20	32		Vendor SN
Page00 172(ACh)	0x20	32		Vendor SN
Page00 173(ADh)	0x20	32		Vendor SN
Page00 174(AEh)	0x20	32		Vendor SN
Page00 175(AFh)	0x20	32		Vendor SN
Page00 176(B0h)	0x20	32		Vendor SN
Page00 177(B1h)	0x02	32		Vendor SN
Page00 178(B2h)	0x20	32		Vendor SN
Page00 179(B3h)	0x20	32		Vendor SN
Page00 180(B4h)	0x20	32		Vendor SN
Page00 181(B5h)	0x20	32		Vendor SN
Page00 182(B6h)	0x32	50	2	Date Code
Page00 183(B7h)	0x32	50	2	Date Code
Page00 184(B8h)	0x30	48	0	Date Code
Page00 185(B9h)	0x39	57	9	Date Code
Page00 186(BAh)	0x30	48	0	Date Code
Page00 187(BBh)	0x31	49	1	Date Code
Page00 188(BCh)	0x30	48	0	Date Code
Page00 189(BDh)	0x31	49	1	Date Code
Page00 190(BEh)	0x00	0		CLEI Code
Page00 191(BFh)	0x00	0		CLEI Code
Page00 192(C0h)	0x00	0		CLEI Code
Page00 193(C1h)	0x00	0		CLEI Code
Page00 194(C2h)	0x00	0		CLEI Code
Page00 195(C3h)	0x00	0		CLEI Code
Page00 196(C4h)	0x00	0		CLEI Code

Page00 197(C5h)	0x00	0		CLEI Code
Page00 198(C6h)	0x00	0		CLEI Code
Page00 199(C7h)	0x00	0		CLEI Code
Page00 200(C8h)	0xE0	224	?	Module Power Characteristics
Page00 201(C9h)	0x78	120	]	Module Power Characteristics
Page00 202(CAh)	0x00	0		Cable assembly length
Page00 203(CBh)	0x00	0		Media Connector Type
Page00 204(CCh)	0x00	0		Copper Cable Attenuation
Page00 205(CDh)	0x00	0		Copper Cable Attenuation
Page00 206(CEh)	0x00	0		Copper Cable Attenuation
Page00 207(CFh)	0x00	0		Copper Cable Attenuation
Page00 208(D0h)	0x00	0		Copper Cable Attenuation
Page00 209(D1h)	0x00	0		Copper Cable Attenuation
Page00 210(D2h)	0x00	0		Cable Assembly Lane Information
Page00 211(D3h)	0x00	0		Cable Assembly Lane Information
Page00 212(D4h)	0x00	0		Media Interface Technology
Page00 213-220 (D5h-DCh)	0x00	0		Reserved
Page00 221(DDh)	0x00	0		Custom
Page00 222(DEh)	0x50	80		Checksum
Page00 223 (DFh)	0x00	0		Custom Info NV
Page00 224 (E0h)				Unique ID
Page00 225-255 (E1h-FFh)	0x00	0		
Page01 128(80h)	0x00	0		Inactive Major FW Rev
Page01 129(81h)	0x00	0		Inactive Minor FW Rev
Page01 130(82h)	0x04	4		Module Major HW Rev
Page01 131(83h)	0x01	1		Module Minor HW Rev
Page01 132(84h)	0x00	0		link length SMF
Page01 133(85h)	0x00	0		link length (OM5)
Page01 134(86h)	0x00	0		link length (OM4)
Page01 135(87h)	0x00	0		link length (OM3)

Page01 136(88h)	0x00	0		link length (OM2)
Page01 137(89h)	0x00	0		Reserved
Page01 138(8Ah)	0x00	0		Nominal Wavelength
Page01 139(8Bh)	0x00	0		Nominal Wavelength
Page01 140(8Ch)	0x00	0		Wavelength Tolerance
Page01 141(8Dh)	0x00	0		Wavelength Tolerance
Page01 142(8Eh)	0x24	36		Implemented Management Interface features advertising
Page01 143(8Fh)	0xDF	223	?	Implemented Management Interface features advertising
Page01 144(90h)	0x57	87		Implemented Management Interface features advertising
Page01 145(91h)	0x04	4		Module Characteristics advertising
Page01 146(92h)	0x55	85	U	Module Characteristics advertising
Page01 147(93h)	0xD8	216	?	Module Characteristics advertising
Page01 148(94h)	0x00	0		Module Characteristics advertising
Page01 149(95h)	0x00	0		Module Characteristics advertising
Page01 150(96h)	0x91	145	?	Module Characteristics advertising
Page01 151(97h)	0x00	0		Module Characteristics advertising
Page01 152(98h)	0x00	0		Module Characteristics advertising
Page01 153(99h)	0xF0	240		RXOUT Amplitude levels supported
Page01 154(9Ah)	0x77	119		RXOUT post and pre-cursor value supported
Page01 155(9Bh)	0x01	1		Implemented Controls advertising
Page01 156(9Ch)	0x03	3		Implemented Controls advertising
Page01 157(9Dh)	0x00	0		Implemented Flags advertising
Page01 158(9Eh)	0x00	0		Implemented Flags advertising
Page01 159(9Fh)	0x23	35	#	Implemented Monitors advertising
Page01 160(A0h)	0x00	0		Implemented Monitors advertising
Page01 161(A1h)	0x08	8		Implemented Signal Integrity Controls advertising
Page01 162(A2h)	0x1C	28		
Page01 163(A3h)	0x00	0		CDB Advertisment
Page01 164(A4h)	0x00	0		CDB Advertisment
Page01 165(A5h)	0x00	0		CDB Advertisment

Page01 166(A6h)	0x00	0		CDB Advertisment
Page01 167(A7h)	0x33			Encoded Maximum Duration ModulePwrDn/Up
Page01 168-175(A8h-AFh)	0x00	0		
Page01 176(B0h)	0x01	1		
Page01 177(B1h)	0x11	17		
Page01 178(B2h)	0x01	1		
Page01 179(B3h)	0x01	1		
Page01 180(B4h)	0x01	1		
Page01 181(B5h)	0x11	17		
Page01 182(B6h)	0xFF	255		
Page01 183(B7h)	0xFF	255		
Page01 184(B8h)	0xFF	255		
Page01 185(B9h)	0xFF	255		
Page01 186(BAh)	0x11	17		Media Lane Assignment Options AppSel code 11
Page01 187-222(BBh-DEh)	0x00			
Page01 223(DFh)	0x4B			Host Interface ID AppSel code 9
Page01 224(E0h)	0xBF			Media Interface ID AppSel code 9
Page01 225(E1h)	0x11			Host and Media Lane Count AppSel code 9
Page01 226(E2h)	0xFF			Host Lane Assignment Options AppSel code 9
Page01 227(E3h)	0x4C			Host Interface ID AppSel code 10
Page01 228(E4h)	0xBF			Media Interface ID AppSel code 10
Page01 229(E5h)	0x11			Host and Media Lane Count AppSel code 10
Page01 230(E6h)	0xFF			Host Lane Assignment Options AppSel code 10
Page01 231(E7h)	0x41			Host Interface ID AppSel code 11
Page01 232(E8h)	0xBF			Media Interface ID AppSel code 11
Page01 233(E9h)	0x44			Host and Media Lane Count AppSel code 11
Page01 234(EAh)	0x11			Host Lane Assignment Options AppSel code 11
Page01 235(EBh)	0xFF			End of applications
Page01 236-254(ECh-FEh)	0x00			

Page01 255(FFh)	0x23	35		Checksum
Page02 128(80h)	0x50	80	–	Temperature monitor high alarm threshold MSB
Page02 129(81h)	0x00	0		Temperature monitor high alarm threshold LSB
Page02 130(82h)	0x00	0		Temperature monitor low alarm threshold MSB
Page02 131(83h)	0x00	0		Temperature monitor low alarm threshold LSB
Page02 132(84h)	0x46	70	U	Temperature monitor high warning threshold MSB
Page02 133(85h)	0x00	0		Temperature monitor high warning threshold LSB
Page02 134(86h)	0x05	5		Temperature monitor low warning threshold MSB
Page02 135(87h)	0x00	0		Temperature monitor low warning threshold LSB
Page02 136(88h)	0x8C	140	?	Supply 3.3-volt monitor high alarm threshold MSB
Page02 137(89h)	0xA0	160	?	Supply 3.3-volt monitor high alarm threshold LSB
Page02 138(8Ah)	0x75	117	u	Supply 3.3-volt monitor low alarm threshold MSB
Page02 139(8Bh)	0x30	48	0	Supply 3.3-volt monitor low alarm threshold LSB
Page02 140(8Ch)	0x8A	138	?	Supply 3.3-volt monitor high warning threshold MSB
Page02 141(8Dh)	0xAC	172	?	Supply 3.3-volt monitor high warning threshold LSB
Page02 142(8Eh)	0x77	119	w	Supply 3.3-volt monitor low warning threshold MSB
Page02 143(8Fh)	0x24	36	$	Supply 3.3-volt monitor low warning threshold LSB
Page02 144-254 (90h-FEh)	0x00	0		
Page02 255(FFh)	3D	61		Checksum
Page03 129(81h)	0x00	0		
Page03 130(82h)				LCD Presence
Page03 131(83h)	0x00	0		User EEPROM
Page03 132(84h)				Insertion Counter MSB
Page03 133(85h)				Insertion Counter LSB
Page03 134(86h)	0x64	100	d	Cut-Off temperature
Page03 135(87h)	0x00	0		Power control registers
Page03 136(88h)	0x00	0		

Page03 137(89h)	0x00	0		
Page03 138(8Ah)	0x00	0		
Page03 139(8Bh)				LPMode/ModSelL State/Edge Detection
Page03 140(8Ch)				IntL Control Register
Page03 141(8Dh)	0x13	19		
Page03 142(8Eh)	0x88	136		
Page03 143(8Fh)				Internally measured Temperature T.S.1 MSB
Page03 144(90h)				Internally measured Temperature T.S.1 LSB
Page03 145-255(91h-FFh)	0x00	0		User EEPROM

2.2.4 Memory Accessibility

The Memory Map registers types are shown in the table below:

Page Address	Address Range	Type
Lower Page	0-25	RO
	26	RW (VR)
	27-126	RO
	127	RW (VR)
Page 00h	128-165	RO
	166-181	RW (NVR)
	182-255	RO
Page 01h	128-255	RO
Page 02h	128-255	RO
Page 03	128-129	RW (NVR)
	130	RO
	131	RW (NVR)
	132-133	RO
	134-140	RW (NVR)
	141	RW
	142-149	RW (NVR)
	150-155	RO
	156-255	RW (NVR)
Page 10h	128-255	RW (VR)
Page 13h	128-143	RO
	144-255	RW (VR)
Page 14h	128	RW (NVR)
	129-255	RO (VR)
Page B0h-B7h	128-255	RW (NVR)
Page B8h	128-255	RW (NVR)

2.3 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- ModselL
- ResetL
- LPMode
- IntL
- ModPrstL

2.3.1 ModselL

The ModSelL is an input signal to the module that is pulled up to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module will not respond to or acknowledge any 2-wire interface communication from the host.

2.3.2 ResetL

ResetL, is an active-low signal, and must be asserted for longer than the minimum reset pulse duration to trigger a module reset.

2.3.3 LPMode

LPMode is an input signal to the module from the host, operating with active high logic. The LPMode signal is pulled up to Vcc in the QSFP-DD module through a 4.75 KOhm resistor. The LPMode signal intervenes in the Module State Transition (refer to section 2.4.2 for more details).

2.3.4 IntL

IntL is an output signal. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The IntL signal is de-asserted “High” after all set interrupt flags are read (IntL pin is open drain, it is pulled high by a pull-up resistor on the Host side).

2.3.5 ModPrstL

ModPrsL is grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and reasserted “High” when the module is physically absent from the host connector.

2.4 ML4062-ALB1-2A/B-112 Specific Functions

2.4.1 Module State

The Module State describes module-wide behaviors and properties. The **ML4062-ALB1-2A/B-112** implements two module states: ModuleLowPwr and ModuleReady.
The ModuleLowPwr state is a host control state, where the management interface is fully initialized and operational and the Module is in Low Power mode, where the Power Spots are deactivated. During this state, the host may configure the module using the management interface and memory map. The module state encoding for ModuleLowPwr is 001.
The ModuleReady state is a host control state that indicates that the module is in High Power mode, and the PWM is activated. The module state encoding for ModuleReady is 011.

Address	Bit	Name	Description	Type
LowMem Reg 3	3~1	Module State	Current state of Module: 001b= ModuleLowPwr 011b= ModuleReady	RO

2.4.2 Module State Transition

The state transition between Low-Power and High-Power is related to three parameters:

1. LowPwrRequestSW bit– software control (forces module into low power mode), register 26 bit 4
2. LowPwrAllowRequestHW bit – software control, register 26 bit 6
3. LPMode – Hardware signal

According to these parameters, the state of the module is defined. Conditions for low-power and high-power state are summarized in the table below.

LowPwrRequestSW (LowMem Reg 26 bit 4)	LowPwrAllowRequestHW (LowMem Reg 26 bit 4)	LPMode	State
1	X	X	Low Power
0	1	1	Low Power
0	1	0	High Power
0	0	1	High Power
0	0	0	High Power

2.4.3 Module Global Controls

Module global controls are control aspects that are applicable to the entire module or all channels in the module.

Address	Bit	Name	Description	Type
LowMem 26	6	LowPwrAllowRequestHW	Parameter used to control the module power mode (refer to section 2.4.2) Default value =1	RW
	4	LowPwrRequestSW	0b = high power mode(default) 1b =Forces module into low power mode	

	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit is self-clearing. 0b = not in reset 1b = Software reset	
LowMem 3	0	Software Interrupt	Digital state of Interrupt: 0b = Interrupt source is present 1b = No interrupt source present	RO

2.4.4 Temperature Monitor

The **ML4062-ALB1-2A/B-112** has 3 internal temperature sensors. Two of them are on the PCBA bottom layer to continuously monitor the module temperature, and the third one is internal to the Retimer Chip to continuously monitor the chip temperature. Internally measured Module temperatures are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius, yielding a total range of –127°C to +128°C that is considered valid between –40° and +125° C.

Address	Bit	Name	Description	Type
Page03 143	All	Temperature MSB	Internally measured TempSense1 (PCB Bottom)	RO
Page03 144	All	Temperature LSB		
LowMem 14	All	Temperature MSB	Internally measured TempSense2 (PCB Bottom)	
LowMem 15	All	Temperature LSB		
LowMem 24	All	Temperature MSB	Retimer Chip Internal Temperature Sensor	
LowMem 25	All	Temperature LSB		

The distribution of internal temperature sensors is shown in the figure below.

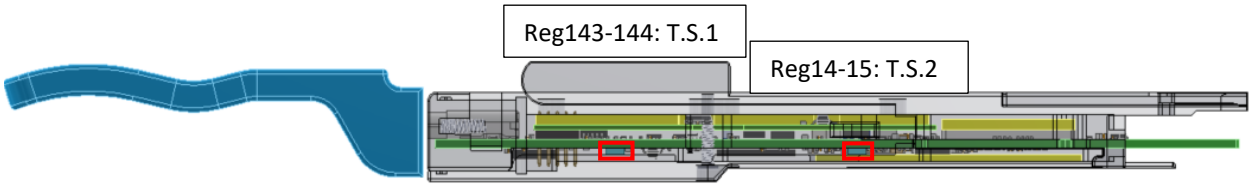

Figure 5: Temperature sensors location

The temperature alarms and warnings interrupt flags exist in lower page.

Address	Bit	Name	Description	Type
LowMem 9	3	L-Temp Low Warning	Latched low temperature warning flag	RO
	2	L-Temp High Warning	Latched high temperature warning flag	
	1	L-Temp Low Alarm	Latched low temperature alarm flag	
	0	L-Temp High Alarm	Latched high temperature alarm flag	

Note that any interrupt flag when asserted will generate the interrupt. Its state is read from LowMem Register 3 bit 0.

2.4.5 Voltage Sense

A voltage sense circuit is available in the **ML4062-ALB1-2A/B-112** that allows to measure the internal module supplied voltage Vcc, with LSB unit is 0.1 mV.

Address	Bit	Name	Description	Type
LowMem 16	All	Supply voltage MSB	Internally measured supply voltage	RO
LowMem 17	All	Supply voltage LSB	Internally measured supply voltage	

The Voltage alarms and warnings interrupt flags exists in lower page.

Address	Bit	Name	Description	Type
LowMem 9	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag	RO
	6	L-Vcc3.3v High Warning	Latched low 3.3 volts supply voltage warning flag	
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag	
	4	L-Vcc3.3v High Alarm	Latched low 3.3 volts supply voltage alarm flag	

2.4.6 Programmable Power Dissipation and Thermal Emulation

The power spots are distributed on a separate board, a daughter card that is mounted on the PCBA, which contains only the power spots.
The daughter card contains three thermal spots that are heated relative to the related control registers settings. The distribution of these spots is shown in the image below (Figure6).

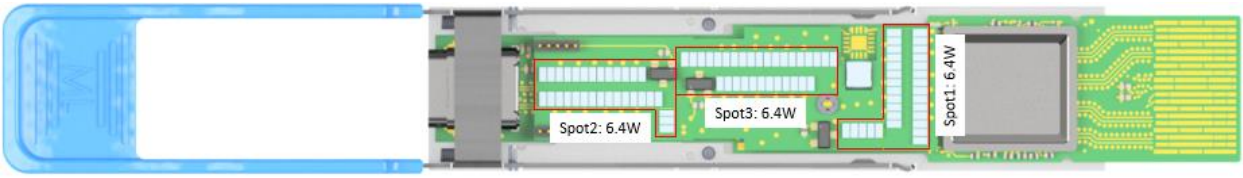

Figure 6: Thermal spots distribution

Registers 135, 136, and 137 Page 03 are used to control thermal spots over I2C. They are 8-bits data wide registers.
The consumed power changes accordingly when the values of these registers are changed (only in high power mode). In Low-power mode the module automatically turns off all power spots. The values written in these registers are permanently stored.

The control registers of the thermal spots are shown in the table below:

Address	Bit	Name	Description	Memory Type
Page03 135	7:0	PWM Controller 1	6.4W power spot PWM Control Register (P3V3_Spots)	RW (NVR)
Page03 136	7:0	PWM Controller 2	6.4 W power spot PWM Control Register (P3V3_Spots)	
Page03 137	7:0	Static Control	6.4 W power spot PWM Control Register (P3V3_Spots)	

Figure 7 shows a side view of the distribution of thermal spots and TIM. The yellow shapes are TIM for heat conduction to the shell. The TIM conductivity is 3 W/m.K.

Figure 7: Module side view

2.4.7 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.
The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, all power spots will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, the PWM goes back to its previous value.
The **ML4062-ALB1-2A/B-112** is set to its maximum Cut-Off temperature of 85°C by default, and can be programmed to any value from register 134 of memory page 03.

Address	Bit	Name	Description	Type
Page03 134	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1 degC	RW (NVR)

2.4.8 Insertion counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved. The insertion counter can be read from registers 132-133 Page03.

Address	Bit	Name	Description	Type
Page03 132	MSB	Insertion Counter MSB		RO
Page03 133	LSB	Insertion Counter LSB	LSB unit = 1 insertion	

2.4.9 Alarm and warning thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory-preset values allow you to determine when a particular value is

exceeding the predefined limit. While Voltage LSB unit is 100 µV and Temperature LSB unit is 1/256 ˚C. Note that these addresses are of memory Page02.

Address	Bit	Name	Default Value	Type
Page02 128	ALL	high temp alarm threshold (MSB)	80˚C	RO
Page02 129	ALL	high temp alarm threshold (LSB)		
Page02 130	ALL	low temp alarm threshold (MSB)	0° C	
Page02 131	ALL	low temp alarm threshold (LSB)		
Page02 132	ALL	high temp warning threshold (MSB)	70˚C	
Page02 133	ALL	high temp warning threshold (LSB)		
Page02 134	ALL	low temp warning threshold (MSB)	5˚C	
Page02 135	ALL	low temp warning threshold (LSB)		
Page02 136	ALL	high volt alarm threshold (MSB)	3.6 V	
Page02 137	ALL	high volt alarm threshold (LSB)		
Page02 138	ALL	low volt alarm threshold (MSB)	3.0 V	
Page02 139	ALL	low volt alarm threshold (LSB)		
Page02 140	ALL	high volt warning threshold (MSB)	3.55 V	
Page02 141	ALL	high volt warning threshold (LSB)		
Page02 142	ALL	low volt warning threshold (MSB)	3.05 V	
Page02 143	ALL	low volt warning threshold (LSB)		

2.4.10 FW and HW Revision

Information about the FW and HW revision are present in Lower Page, registers 39-40, and in page 01 registers 130-131, respectively, as described in the table below.

Address	Bit	Description	Type
LowMem 39	All	Major FW Rev	RO
LowMem 40	All	Minor FW Rev	
Page01 130	All	Major HW Rev	
Page01 131	All	Minor HW Rev	

2.4.11 Status Register

Register 139 of page 3 reports the digital state of the QSFP-DD low speed signals.

Address	Bit	Name	Description	Type
Page03 139	0	ModSel	Digital state of ModSel pin	RO
	1	LPMode	Digital state of LPMode	

Note that when the ModSelL is High the I2C will stop working and the user will read FF from register 139.

2.4.12 Digital State Detection

The module must be able to detect the digital state of the LPMode and ModSelL signals. An I2C latch register in upper page 03 is latched on both rising and falling edges of the LPMode and ModSelL signals.

Address	Bit	Name	Description	Type
Page03 139	4	ModSelL transection	Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW
	5	LPMode transection		

2.4.13 Digital Control of IntL

During power-up of the module, IntL is defaulted to negated. The host can then set the status of this signal to any status through register 140 in upper page 03.

Address	Bit	Name	Description	Type
Page03 140	2	IntL control	00xb: Normal operation 010b: Force IntL to logic 0, VIntL < Vol(max) 011b: Force IntL to logic 1, VIntL > Voh(min) 1xxb: IntL is tri-stated	RW (NVR)
	1			
	0			

3 High Speed

The **ML4062-ALB1-2A/B-112** includes a low power 800G retimer transceiver chip. The transceiver operates at 53.125 PAM4, Gray coded pattern. The default mode of operation is the retimed loopback mode.

3.1 Supported Rates

Application Bit Rate, Gb/s[2]	Lane Count	Lane Signaling Rate, GBd[2]	Modulation	AppSel Code	Application
850	8	53.125	PAM4	**1**	800G S C2M
425	4	53.125	PAM4	**2**	400GAUI-4-S C2M
425	8	26.5625	PAM4	3	400GAUI-8 C2M
212.50	8	26.5625	NRZ	4	200GAUI-8 C2M
850	8	53.125	PAM4	5	800G L C2M
425	4	53.125	PAM4	6	400GAUI-4-L C2M
53.13	1	26.5625	PAM4	7	50GAUI-1 C2M
25.78	1	25.78125	NRZ	8	25GAUI C2M
106.25	1	53.125	PAM4	9	100GAUI-1-S C2M
106.25	1	53.125	PAM4	10	100GAUI-1-L C2M
103.13	4	25.78125	NRZ	11	CAUI-4 C2M (Annex 83E) without FEC
Custom	Customizable	25.78125	PAM4		
Custom	Customizable	41.25	PAM4		
Custom	Customizable	41.25	NRZ		
Custom	Customizable	51.5625	PAM4		
Custom	Customizable	51.5625	NRZ		
Custom	Customizable	53.125	NRZ		
Custom	Customizable	56.25	PAM4		
Custom	Customizable	56.25	NRZ		
Custom	Customizable	55.904735	PAM4		
Custom	Customizable	56.152354	PAM4		
Custom	Customizable	28.076177	PAM4		
Custom	Customizable	53.247670	PAM4		

3.2 Advertisement

3.2.1 Supported AppSel Codes

This paragraph lists the module supported AppSel codes.

Address	Name	Description	Default Value
LowMem 85	Media Type	The MediaType field defines the interpretation of MediaInterfaceID values in the following Application Descriptors. In this application it indicates "Active Cables"	0x04
LowMem 86	Host Interface ID AppSel code 1	Host Electrical Interface ID, 800G S C2M	0x51
LowMem 87	Media Interface ID AppSel code 1	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
LowMem 88	Host and Media Lane Count AppSel code 1	8 host lanes and 8 media lanes	0x88
LowMem 89	Host Lane Assignment Options AppSel code 1	Application begin on the host lane 1	0x01
LowMem 90	Host Interface ID AppSel code 2	Host Electrical Interface ID, 400GAUI-4-S C2M	0x4F
LowMem 91	Media Interface ID AppSel code 2	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
LowMem 92	Host and Media Lane Count AppSel code 2	4 host lanes and 4 media lanes	0x44
LowMem 93	Host Lane Assignment Options AppSel code 2	Application begin on the host lane 1 and 5	0x11
LowMem 94	Host Interface ID AppSel code 3	Host Electrical Interface ID, 400GAUI-8 C2M	0x11
LowMem 95	Media Interface ID AppSel code 3	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
LowMem 96	Host and Media Lane Count AppSel code 3	8 host lanes and 8 media lanes	0x88
LowMem 97	Host Lane Assignment Options AppSel code 3	Application begin on the host lane 1	0x01
LowMem 98	Host Interface ID AppSel code 4	Host Electrical Interface ID, 200GAUI-8 C2M	0x0E
LowMem 99	Media Interface ID AppSel code 4	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
LowMem 100	Host and Media Lane Count AppSel code 4	8 host lanes and 8 media lanes	0x88
LowMem 101	Host Lane Assignment Options AppSel code 4	Application begin on the host lane 1	0x01
LowMem 102	Host Interface ID AppSel code 5	Host Electrical Interface ID, 800G L C2M	0x52
LowMem 103	Media Interface ID AppSel code 5	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
LowMem 104	Host and Media Lane Count AppSel code 5	8 host lanes and 8 media lanes	0x88

LowMem 105	Host Lane Assignment Options AppSel code 5	Application begin on the host lane 1	0x01
LowMem 106	Host Interface ID AppSel code 6	Host Electrical Interface ID, 400GAUI-4-L C2M	0x50
LowMem 107	Media Interface ID AppSel code 6	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
LowMem 108	Host and Media Lane Count AppSel code 6	4 host lanes and 4 media lanes	0x44
LowMem 109	Host Lane Assignment Options AppSel code 6	Application begin on the host lane 1 and 5	0x11
LowMem 110	Host Interface ID AppSel code 7	Host Electrical Interface ID, 50GAUI-1 C2M	0x0A
LowMem 111	Media Interface ID AppSel code 7	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
LowMem 112	Host and Media Lane Count AppSel code 7	1 host lane and 1 media lane	0x11
LowMem 113	Host Lane Assignment Options AppSel code 7	Application can begin on any host lane	0xFF
LowMem 114	Host Interface ID AppSel code 8	Host Electrical Interface ID, 25GAUI C2M	0x05
LowMem 115	Media Interface ID AppSel code 8	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
LowMem 116	Host and Media Lane Count AppSel code 8	1 host lane and 1 media lane	0x11
LowMem 117	Host Lane Assignment Options AppSel code 8	Application can begin on any host lane	0xFF
Page 01h 223	Host Interface ID AppSel code 9	Host Electrical Interface ID, 100GAUI-1-S C2M	0x4B
Page 01h 224	Media Interface ID AppSel code 9	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
Page 01h 225	Host and Media Lane Count AppSel code 9	1 host lane and 1 media lane	0x11
Page 01h 226	Host Lane Assignment Options AppSel code 9	Application begin on any host lane	0xFF
Page 01h 227	Host Interface ID AppSel code 10	Host Electrical Interface ID, 100GAUI-1-L C2M	0x4C
Page 01h 228	Media Interface ID AppSel code 10	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
Page 01h 229	Host and Media Lane Count AppSel code 10	1 host lane and 1 media lane	0x11
Page 01h 230	Host Lane Assignment Options AppSel code 10	Application begin on any host lane	0xFF
Page 01h 231	Host Interface ID AppSel code 11	Host Electrical Interface ID, CAUI-4 C2M (Annex 83E) without FEC	0x41
Page 01h 232	Media Interface ID AppSel code 11	Media Interface ID, Active Loopback module as per SFF-8024 V4.9	0xBF
Page 01h 233	Host and Media Lane Count AppSel code 11	4 host lanes and 4 media lanes	0x44
Page 01h 234	Host Lane Assignment Options AppSel code 11	Application begin on the host lane 1 and 5	0x11

Page 01h 235	End of Applications		This indicates end of AppSel codes advertisement	0xFF
Page 01h 153	**Bit 7**	RxOutputLevel3Supported	0b/1b: Amplitude Code 3 not supported/supported	1
	Bit 6	RxOutputLevel2Supported	0b/1b: Amplitude Code 3 not supported/supported	1
	Bit 5	RxOutputLevel1Supported	0b/1b: Amplitude Code 3 not supported/supported	1
	Bit 4	RxOutputLevel0Supported	0b/1b: Amplitude Code 3 not supported/supported	1
Page 01h 154	**Bit 7-4**	RxOutputEqPostCursorMax	Maximum supported value of the Rx Output Eq Post-cursor control	0x7
	Bit 3-0	RxOutputEqPreCursorMax	Maximum supported value of the Rx Output Eq Pre-cursor control	0x7
Page 01h 162	**Bit 4-3**	RxOutputEqControlSupported	00b: Rx Output Eq control not supported 01b: Rx Output Eq Pre-cursor control supported 10b: Rx Output Eq Post-cursor control supported 11b: Rx Output Eq Pre- and Post-cursor control supported	11
	Bit 2	RxOutputAmplitudeControlSupported	0b: Rx Output Amplitude control not supported 1b: Rx Output Amplitude control supported	1
Page 01h 176	MediaLaneAssignmentOptionsApp1		Media Lane Assignment Options for the Application advertised in Application descriptor identified by AppSel <i>. Bits 0-7 form a bit map corresponding to Media Lanes 1-8. A set bit indicates that a Data Path for the Application is allowed to begin on the corresponding Media Lane. Each instance of an Application uses contiguous Media Lane numbers. If multiple instances of a single Application are allowed, each starting point is identified, and all instance must be supported concurrently.	0x01
Page 01h 177	MediaLaneAssignmentOptionsApp2			0x01
Page 01h 178	MediaLaneAssignmentOptionsApp3			0x01
Page 01h 179	MediaLaneAssignmentOptionsApp4			0x01

3.2.2 Supported Features and Capabilities

This paragraph lists the module supported features and capabilities. All registers mentioned in the table below are present in **Page 13h**.

Address	Bit	Name	Description	Default Value	Type
Page 13h 128	4	PerLaneHostSideLoopbacks	0b: Not supported 1b: Supported	0	RO
	3	HostSideInputLoopback	0b: Not supported 1b: Supported	1	

Page 13h 129	7-6	GatingSupport	0: Not Supported 1: Supported with time accuracy <= 2 ms 2: Supported with time accuracy <= 20 ms 3: Supported with time accuracy > 20 ms	0	RO
	5	GatingResultsSupported	Gating result statistics selectable by diagnosticsSelector (14h:128) values 11h-15h are: 0b: Not supported 1b: Supported	0	
	4	PeriodicUpdatesSupported	Realtime statistics selectable by DiagnosticsSelector (14h:128) values 01h-06h are periodically updated during measurement: 0b: no periodic update during measurement 1b: periodic update during measurement	1	
	3	PerLaneGatingTimersSupported	0b: Only two global gating timers are available for all lanes on all Banks, one for Host Side Measurements and one for Media Side Measurements. 1: Per lane gating timers are supported in all Banks	0	
	2	AutoRestartGatingSupported	0b: AutoRestartGating control (13h:177.4) not supported 1b: AutoRestartGating control (13h:177.4) supported	0	
Page 13h 130	4	HostSideInputSNRMeasurement	Indicates if hos side SNR measurement reported via Diagnostics Selection value 06h is supported (Byte 14h:128) 1b: Supported 0b: Not supported	1	RO
	1	BitsAndErrorsCountingSupported	Indicates if DiagnosticsSelector values 02h-05h are supported (Page 14h byte 128, Table 8-114) 0b: Not supported 1b: Supported	1	
Page 13h 131	2	PRBSGeneratorHostSidePostFEC	0b: Not supported 1b: Supported	1	RO
	1	PRBSCheckerHostSidePreFEC	0b: Not supported 1b: Supported	1	
Page 13h 132	7	HostSideGeneratorSupportsPattern7	PRBS-13 (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	0	RO
	6	HostSideGeneratorSupportsPattern6	PRBS-13Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	1	
	5	HostSideGeneratorSupportsPattern5	PRBS-15 (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	0	

	4	HostSideGeneratorSupportsPattern4	PRBS-15Q (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	1	
	3	HostSideGeneratorSupportsPattern3	PRBS-23 (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	0	
	2	HostSideGeneratorSupportsPattern2	PRBS-23Q (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	1	
	1	HostSideGeneratorSupportsPattern1	PRBS-31 (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	0	
	0	HostSideGeneratorSupportsPattern0	PRBS-31Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	1	
Page 13h 133	7	HostSideGeneratorSupportsPattern15	User Pattern (Programmable pattern provided in Bytes 13h:224-255): 0b: Not supported 1b: Supported	1	RO
	6	HostSideGeneratorSupportsPattern14	Custom Vendor defined pattern	1	
	5	HostSideGeneratorSupportsPattern13	Reserved	0	
	4	HostSideGeneratorSupportsPattern12	SSPRQ (As defined in IEEE 802.3-2018 clause 120.5.11.2.3)	1	
	3	HostSideGeneratorSupportsPattern11	PRBS-7 (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	0	
	2	HostSideGeneratorSupportsPattern10	PRBS-7Q (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	1	
	1	HostSideGeneratorSupportsPattern9	PRBS-9 (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	0	
	0	HostSideGeneratorSupportsPattern8	PRBS-9Q (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	1	
Page 13h 136	7	HostSideCheckerSupportsPattern7	PRBS-13 (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	0	RO
	6	HostSideCheckerSupportsPattern6	PRBS-13Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	1	
	5	HostSideCheckerSupportsPattern5	PRBS-15 (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	0	
	4	HostSideCheckerSupportsPattern4	PRBS-15Q (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	1	

	3	HostSideCheckerSupportsPattern3	PRBS-23 (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	0	
	2	HostSideCheckerSupportsPattern2	PRBS-23Q (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	1	
	1	HostSideCheckerSupportsPattern1	PRBS-31 (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	0	
	0	HostSideCheckerSupportsPattern0	PRBS-31Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	1	
Page 13h 137	7	HostSideCheckerSupportsPattern15	User Pattern (Programmable pattern provided in Bytes 13h:224-255): 0b: Not supported 1b: Supported	0	RO
	6	HostSideCheckerSupportsPattern14	Custom Vendor defined pattern	0	
	5	HostSideCheckerSupportsPattern13	Reserved	0	
	4	HostSideCheckerSupportsPattern12	SSPRQ (As defined in IEEE 802.3-2018 clause 120.5.11.2.3)	0	
	3	HostSideCheckerSupportsPattern11	PRBS-7 (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	0	
	2	HostSideCheckerSupportsPattern10	PRBS-7Q (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	1	
	1	HostSideCheckerSupportsPattern9	PRBS-9 (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	0	
	0	HostSideCheckerSupportsPattern8	PRBS-9Q (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	1	
Page 13h 140	7-6	RecoveredClockForGeneratorOptions	Options to use recovered clock for contra-directional pattern generator on the same module side: 00b: not supported 01b: supported without loopback 10b: supported with loopback 11b: supported with and without loopback	0b10	RO
	5	ReferenceClockForPatternsSupported	option to use reference clock for pattern generation: 0b: Not supported 1b: Supported	1	
	3-0	UserPatternLengthSupported	Maximum length L of the user defined pattern, where the field value n encodes L as L=2(n+1), i.e. 0000b: 2 bytes, …, 1111b: 32 bytes	0b0111	

Page 13h 141	3	HostSideCheckerSupportsDataSwap	Register 162 for swapping the MSB and LSB for PAM4 patterns: 0b: Not supported 1b: Supported	0	RO
	2	HostSideCheckerSupportsDataInvert	Register 161 for pattern inversion: 0b: Not supported 1b: Supported	0	
	1	HostSideGeneratorSupportsDataSwap	Register 146 for swapping the MSB and LSB for PAM4 patterns: 0b: Not supported 1b: Supported	0	
	0	HostSideGeneratorSupportsDataInvert	Register 145 for pattern inversion: 0b: Not supported 1b: Supported	0	
Page 13h 142	3	HostCheckerSupportsPerLaneEnable	Host Side pattern checker for lane i enabled in 13h:160 enables lane i 0b: per lane enable not supported 1b: per lane enable supported	1	RO
	2	HostCheckerSupportsPerLanePattern	Host Side pattern selection for checker 0b: Lane 1 Pattern Type 13h:164.3-0 is used for all lanes. 1b: Per lane Pattern selection 13h:164-167	1	
	1	HostGeneratorSupportsPerLaneEnable	Host Side pattern generator for lane i enabled in 13h:144 enables lane i 0b: per lane enable not supported 1b: per lane enable supported	1	
	0	HostGeneratorSupportsPerLanePattern	Host Side pattern selection for generator 0b: Lane 1 Pattern 13h:148.3-0 is used for all lanes. 1b: Per lane Pattern selection 13h.148-151	1	

3.3 Lane and Data Path Control (Page 10h), Staged Control Set 0

3.3.1 Data Path Configuration (Application Assignments)

The Data Path Configuration fields allow the host to allocate and configure the Data Paths consisting of one or more lanes for one or more of the Applications advertised by the module in the Application Descriptor registers.
The second table below describes the Data Path Configuration as a DPConfigLane<i> configuration register array.

The first table below describes the fields in a DPConfigLane<i> configuration Byte, two of which are descriptive (AppSelCode and DataPathID), while one (ExplicitControl) optionally customizes standard lane configurations.

Data Path Configuration per Lane (DPConfigLane<i>)

Lane	Bit	Name	Description	Type

<i>	7-4	AppSelCode	If lane <i> is part of a Data Path for an Application instance, the AppSelCode field stores the AppSel code of the Descriptor of that Application (see Table 8-19 and Table 8-52 in CMIS 5.0). If lane <i> is not part of a Data Path for an Application and hence unused, the AppSelCode field is assigned the NULL value 0000b. All lanes of a Data Path for an Application that spans multiple lanes must have the same setting of AppSelCode.	RW
	3-1	DataPathID	If lane <i> is part of a Data Path for an Application instance, this DataPathID field stores the DataPathID of that Data Path, i.e. the number of the first lane in the Data Path, decremented by one. If lane<i> is unused, the value of DataPathID is ignored. All lanes of a Data Path for an Application that spans multiple lanes must have the same setting of DataPathID. *Note: For example, the DataPathID of a Data Path including lane 1 is 0 (000b) and the DataPathID of a Data Path where lane 5 is the lowest lane number is 4 (100b).*	RW
	0	ExplicitControl	If lane <i> is part of a Data Path for an Application instance, the ExplicitControl field specifies if lane <i> is configured with host-defined signal integrity settings (provisioned in registers described in the Table in section 3.2.2) or with Application-dependent settings known by the module, when the Staged Control Set is Applied. If lane <i> is unused, the field is ignored. 0b: Use Application-dependent settings for lane <i> 1b: Use Staged Control Set 0 control values for lane <i>	RW

Staged Control Set 0, Data Path Configuration (Page 10h)

Address	Bit	Name	Description	Default Value	Type
Page10h 145	7-4	AppSelCodeLane1	See the table above	0x01	RW VR
	3-1	DataPathIDLane1		0x00	RW VR
	0	ExplicitControlLane1		0x01	RW VR
Page10h 146	7-4	AppSelCodeLane2	See the table above	0x01	RW VR
	3-1	DataPathIDLane2		0x00	RW VR
	0	ExplicitControlLane2		0x01	RW VR
Page10h 147	7-4	AppSelCodeLane3	See the table above	0x01	RW VR
	3-1	DataPathIDLane3		0x00	RW VR
	0	ExplicitControlLane3		0x01	RW VR
Page10h 148	7-4	AppSelCodeLane4	See the table above	0x01	RW VR
	3-1	DataPathIDLane4		0x00	RW VR
	0	ExplicitControlLane4		0x01	RW VR
Page10h 149	7-4	AppSelCodeLane5	See the table above	0x01	RW VR
	3-1	DataPathIDLane5		0x00	RW VR
	0	ExplicitControlLane5		0x01	RW VR
Page10h 150	7-4	AppSelCodeLane6	See the table above	0x01	RW VR
	3-1	DataPathIDLane6		0x00	RW VR
	0	ExplicitControlLane6		0x01	RW VR
Page10h 151	7-4	AppSelCodeLane7	See the table above	0x01	RW VR
	3-1	DataPathIDLane7		0x00	RW VR
	0	ExplicitControlLane7		0x01	RW VR
	7-4	AppSelCodeLane8	See the table above	0x01	RW VR

Page10h 152	3-1	DataPathIDLane8		0x00	RW VR
	0	ExplicitControlLane8		0x01	RW VR

User can choose to change AppSel code in the Stages Control set by apply either ApplyImmediate or ApplyDPInitLane trigger mentioned above in section 3.2.3 below.

AppSel code 1	→	800G S C2M (placeholder)	Speed: 1x800G
AppSel code 2	→	400GAUI-4-S C2M (Annex 120G)	Speed: 2x400G
AppSel code 3	→	400GAUI-8 C2M (Annex 120E)	Speed: 1x400G
AppSel code 4	→	200GAUI-8 C2M (Annex 120C)	Speed: 1x200G
AppSel code 5	→	800G L C2M (placeholder)	Speed: 1x800G
AppSel code 6	→	400GAUI-4-L C2M (Annex 120G)	Speed: 2x400G
AppSel code 7	→	50GAUI-1 C2M (Annex 135G)	Speed: 8x50G
AppSel code 8	→	25GAUI C2M (Annex 109B)	Speed: 8x25G
AppSel code 9	→	100GAUI-1-S C2M (Annex 120G)	Speed: 8x100G
AppSel code 10	→	100GAUI-1-L C2M (Annex 120G)	Speed: 8x100G
AppSel code 11	→	CAUI-4 C2M (Annex 83E) without FEC	Speed: 8x100G

For more information, refer to section 6.2.4.3 Host Rules and Recommendations in CMIS 5.0.

3.3.2 Tx and Rx Signal Integrity Controls

The following control fields, present in **Page 10h**, allow the host to pre-program signal integrity settings per lane, which the module uses instead of default values that are associated with the Application configured on the Data Path of the lane.

These fields are without effect unless the lane specific ExplicitControl bits are set, as described in CMIS 5.0 section 6.2.3.

These fields have no effect until the staged control set is applied to the Active Control Set.

See CMIS 5.0 section 6.2.3 for the dependency of these fields on the value of the ExplicitControl bit.

See CMIS 5.0 section 6.2.5 for definitions of valid signal integrity control settings.

Staged Control Set 0, Rx Controls (Page 10h)

Address	Bit	Name	Description	Default Values	Type
Page10h 162	7-4	Output EqPreCursor Target Rx2	Rx output equalization pre-cursor target See first table below Advertisement: 01h:162.4-3	0x4	RW VR
	3-0	Output EqPreCursor Target Rx1		0x4	RW VR
Page10h 163	7-4	Output EqPreCursor Target Rx4		0x4	RW VR
	3-0	Output EqPreCursor Target Rx3		0x4	RW VR
Page10h 164	7-4	Output EqPreCursor Target Rx6		0x4	RW VR
	3-0	Output EqPreCursor Target Rx5		0x4	RW VR

Page10h 165	7-4	Output EqPreCursor Target Rx8		0x4	RW VR
	3-0	Output EqPreCursor Target Rx7		0x4	RW VR
Page10h 166	7-4	Output EqPostCursor Target Rx2		0x4	RW VR
	3-0	Output EqPostCursor Target Rx1		0x4	RW VR
Page10h 167	7-4	Output EqPostCursor Target Rx4	Rx output equalization post-cursor target See first table below Advertisement: 01h:162.4-3	0x4	RW VR
	3-0	Output EqPostCursor Target Rx3		0x4	RW VR
Page10h 168	7-4	Output EqPostCursor Target Rx6		0x4	RW VR
	3-0	Output EqPostCursor Target Rx4		0x4	RW VR
Page10h 169	7-4	Output EqPostCursor Target Rx8		0x4	RW VR
	3-0	Output EqPostCursor Target Rx7		0x4	RW VR
Page10h 170	7-4	Output EqAmplitude Target Rx2	Rx output amplitude target See second table below Advertisement: 01h:162.2	0x2	RW VR
	3-0	Output EqAmplitude Target Rx1		0x2	RW VR
Page10h 171	7-4	Output EqAmplitude Target Rx4		0x2	RW VR
	3-0	Output EqAmplitude Target Rx3		0x2	RW VR
Page10h 172	7-4	Output EqAmplitude Target Rx6		0x2	RW VR
	3-0	Output EqAmplitude Target Rx5		0x2	RW VR
Page10h 173	7-4	Output EqAmplitude Target Rx8		0x2	RW VR
	3-0	Output EqAmplitude Target Rx7		0x2	RW VR

Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB

Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)

User can choose to change per lane pre/post-cursor and amplitude using the staged set 0. Apply either ApplyImmediate or ApplyDPInitLane trigger mentioned above in section 3.2.3 below to trigger the change.

For more information, refer to section 6.2.5 (Signal Integrity Related Control) in CMIS 5.0.

3.3.3 Apply Staged Control Set Triggers (Configuration Commands)

SCS0::ApplyDPInit and **SCS0::ApplyImmediate** are write-only (WO) trigger registers that allow the host to request execution of a configuration or reconfiguration procedure for one or more Data Paths selected by means of a lane bit mask in the value being written to the trigger register. *Note: Changes to per-lane configurations of a Staged Control Set have no effect on the behavior of a lane until the host has successfully triggered ApplyDPInit or ApplyImmediate for the lane (causing a copy of the lane configuration in the staged control set into the Active Control Set and, ultimately, into hardware or firmware).*

Note: As described in sections 6.2.3.3, an ApplyDPInit trigger may cause commissioning to hardware without host intervention by a series of DPSM state transitions through DPInit, initiated via the DPInitPending bits.

*Note: ApplyImmediate is not supported when **SteppedConfigOnly**=1, WRITE access is then ignored.*

A successful **Provision** configuration procedure copies settings from a Staged Control Set to the Active Control set and sets DPInitPending bits.

A successful **Provision-and-Commission** reconfiguration procedure copies settings from a Staged Control Set to the Active Control set and commits the Active Control set to hardware.

Note: The ApplyDPInit and ApplyImmediate registers are stateless trigger registers with write-only access type. This implies that the value read from the register is not specified. Modules may use the bits in these registers for any purpose, including to signal command execution or acceptance status, e.g. for debug purposes.

Staged Control Set 0, Apply Triggers (Page 10h)

Address	Bit	Name	Description	Default Value	Type
Page10h 143	0	ApplyDPInitLane1	SCS0::ApplyDPInitLane<i> 0b: No action for host lane <i> 1b: Trigger the Provision procedure using the Staged Control Set 0 settings for host lane <i>, with feedback provided in the associated ConfigStatusLane<i> field Restriction: This byte must be written in a single-byte WRITE	0	WO
	1	ApplyDPInitLane2		0	
	2	ApplyDPInitLane3		0	
	3	ApplyDPInitLane4		0	
	4	ApplyDPInitLane5		0	
	5	ApplyDPInitLane6		0	
	6	ApplyDPInitLane7		0	
	7	ApplyDPInitLane8		0	
Page10h 144	0	ApplyImmediateLane1	SCS0::ApplyImmediate<i> 0b: No action for host lane <i> 1b: Trigger the Provision or the Provision-and-Commission procedure using the Staged Control Set 0 settings for host lane <i>, with feedback provided in the associated ConfigStatusLane<i> field	0	WO
	1	ApplyImmediateLane2		0	
	2	ApplyImmediateLane3		0	
	3	ApplyImmediateLane4		0	
	4	ApplyImmediateLane5		0	
	5	ApplyImmediateLane6		0	
	6	ApplyImmediateLane7		0	

	7	ApplyImmediateLane8	Restriction: This byte must be written in a single-byte WRITE	0	

3.4 Lane and Data Path Status

3.4.1 Data Path States

The following fields report the Data Path States of the Data Path State Machines associated with each host lane.
Data Path States apply to both the host and the media interfaces, but are reported by host lane.
For Data Paths with multiple lanes, the module reports the same state for the lanes of each Data Path.
For unused lanes that are not part of a Data Path, the module reports DPDeactivated.
An indication of DPDeactivated means that no Data Path is initialized on that lane.
The second table below defines the Data Path State encodings.

Lane-associated Data Path States (Page 11h)

Address	Bit	Name	Description	Default Value	Type
Page11h 128	7-4	Data Path State host lane 2	Data Path State of host lane 2 (see table below)	0x01	RO
	3-0	Data Path State host lane 1	Data Path State of host lane 1 (see table below)	0x01	RO
Page11h 129	7-4	Data Path State host lane 4	Data Path State of host lane 4 (see table below)	0x01	RO
	3-0	Data Path State host lane 3	Data Path State of host lane 3 (see table below)	0x01	RO
Page11h 130	7-4	Data Path State host lane 6	Data Path State of host lane 6 (see table below)	0x01	RO
	3-0	Data Path State host lane 5	Data Path State of host lane 5 (see table below)	0x01	RO
Page11h 131	7-4	Data Path State host lane 8	Data Path State of host lane 8 (see table below)	0x01	RO
	3-0	Data Path State host lane 7	Data Path State of host lane 7 (see table below)	0x01	RO

Data Path State Encoding

Encoding	State
0h	Reserved
1h	DPDeactivated (or unused lane)
2h	DPInit
3h	DPDeinit
4h	DPActivated
5h	DPTxTurnOn
6h	DPTxTurnOff
7h	DPInitialized
8h-Fh	Reserved

3.4.2 Lane-Specific Flags

This section of the Memory Map contains lane-specific Flags. These Flags provide a mechanism for reporting lane-specific status changes, operating failures, alarms and warnings for monitored observables, or event occurrences. Each lane-specific Flag has an associated Mask.

The general behavior of Flags, Masks, and Interrupt generation is described in CMIS 5.0 section 8.1.4.2.
The lane-specific Flags, present in **Page 11h**, are defined below.

Address	Bit	Name	Description	Default Value	Type
Page 11h 134	7	DPStateChangedFlag8	Latched Data Path State Changed flag for host lane 8	0	RO/COR
	6	DPStateChangedFlag7	Latched Data Path State Changed flag for host lane 7	0	
	5	DPStateChangedFlag6	Latched Data Path State Changed flag for host lane 6	0	
	4	DPStateChangedFlag5	Latched Data Path State Changed flag for host lane 5	0	
	3	DPStateChangedFlag4	Latched Data Path State Changed flag for host lane 4	0	
	2	DPStateChangedFlag3	Latched Data Path State Changed flag for host lane 3	0	
	1	DPStateChangedFlag2	Latched Data Path State Changed flag for host lane 2	0	
	0	DPStateChangedFlag1	Latched Data Path State Changed flag for host lane 1	0	

3.4.3 Configuration Command Execution and Result Status (ConfigStatus)

As described in CMIS 5.0 sections 6.2.3.3, 6.2.4, and 8.8.3.1, the host can command a configuration procedure to be executed by the module, by writing a lane trigger bit mask to an Apply register in that Staged Control Set where the desired configuration has been defined.

Both the Provisioning procedure and the Provisioning-and-Commissioning procedure may take significant time to execute and may be rejected, for a variety of reasons. Therefore, a synchronization protocol about currently ongoing execution and eventual result feedback is implemented, by means of the Configuration Command Execution and Result Status (ConfigStatus) register (see table below).

The field ConfigStatusLane<i>, present in **Page 11h**, informs the host both on the current command handling status and on 10 the final result status of the most recently accepted configuration command affecting lane <i>.

Configuration Command Status registers (Page 11h)

Address	Bit	Name	Description	Default Value	Type
Page 11h 202	7-4	ConfigStatusLane2	ConfigStatusLane<i> Configuration Command Execution / Result Status for the Data Path of host lane <i>, during and after the most recent configuration command. See below for the encoding of values.	0x1	RO
	3-0	ConfigStatusLane1		0x1	RO
Page 11h 203	7-4	ConfigStatusLane4		0x1	RO
	3-0	ConfigStatusLane3		0x1	RO
Page 11h 204	7-4	ConfigStatusLane6		0x1	RO
	3-0	ConfigStatusLane5		0x1	RO
Page 11h 205	7-4	ConfigStatusLane8		0x1	RO
	3-0	ConfigStatusLane7		0x1	RO

Configuration Command Execution and Result Status Codes (Page 11h)

Encoding	Name	Description
1h	ConfigSuccess	**Positive Result Status**: The last accepted configuration command has been completed successfully
3h	ConfigRejectedInvalidAppSel	Configuration rejected: invalid AppSel code
5h	ConfigRejectedInvalidSI	Configuration rejected: invalid SI control settings

Ch	ConfigInProgress	**Execution Status**: A configuration command is still being processed by the module; a new configuration command is **ignored** for this lane while ConfigInProgress.

3.4.4 Data Path Configuration (Application Assignment)

The following fields allow the host to infer the current baud rate, modulation format, and Data Path width, as well as other interface related specification elements, for each lane in the module.

Data Path Configuration per Lane (DPConfigLane<i> Field)

Lane	Bits	Name	Description	Type
<i>	7-4	AppSelCode	**ACS::AppSelCodeLane<i>** Defines the Application assigned to the Data Path containing lane <i> by reference to the Application Descriptor of that Application: **0000b**: lane <i> is unused and unassigned (not part of a Data Path) **0001b**, …, **1111b**: lane <i> is part of a Data Path for the Application described in Application Descriptor with AppSel code AppSelCodeLane<i>	RO
	3-1	DataPathID	**ACS::DataPathIDLane<i>** Index of first lane in the Data Path containing lane <i> 000b: Lane 1 001b: Lane 2 …. 111b: Lane 8	RO
	0	ExplicitControl	**ACS::ExplicitControlLane<i>** 0b: Lane <i> SI settings are Application dependent 1b: Lane <i> SI settings are host defined	RO

Indicators for Active Control Set, Data Path Configuration (Page 11h)

Address	Bit	Name	Description	Default Value	Type
Page 11h 206	7-4	AppSelCodeLane1	**ACS::DPConfigLane1** See Table above	0x01	RO
	3-1	DataPathIDLane1		0x00	
	0	ExplicitControlLane1		0x01	
Page 11h 207	7-4	AppSelCodeLane2	**ACS::DPConfigLane2** See Table above	0x01	RO
	3-1	DataPathIDLane2		0x00	
	0	ExplicitControlLane2		0x01	
Page 11h 208	7-4	AppSelCodeLane3	**ACS::DPConfigLane3** See Table above	0x01	RO
	3-1	DataPathIDLane3		0x00	
	0	ExplicitControlLane3		0x01	
Page 11h 209	7-4	AppSelCodeLane4	**ACS::DPConfigLane4** See Table above	0x01	RO
	3-1	DataPathIDLane4		0x00	
	0	ExplicitControlLane4		0x01	
Page 11h 210	7-4	AppSelCodeLane5	**ACS::DPConfigLane5** See Table above	0x01	RO
	3-1	DataPathIDLane5		0x00	
	0	ExplicitControlLane5		0x01	
Page 11h 211	7-4	AppSelCodeLane6	**ACS::DPConfigLane6** See Table above	0x01	RO
	3-1	DataPathIDLane6		0x00	
	0	ExplicitControlLane6		0x01	
Page 11h 212	7-4	AppSelCodeLane7	**ACS::DPConfigLane7** See Table above	0x01	RO
	3-1	DataPathIDLane7		0x00	
	0	ExplicitControlLane7		0x01	

Page 11h 213	7-4	AppSelCodeLane8	**ACS::DPConfigLane8** See Table above	0x01	RO
	3-1	DataPathIDLane8		0x00	
	0	ExplicitControlLane8		0x01	

3.4.5 Tx and Rx Signal Integrity Fields

The fields described below, present in **Page 11h**, report the active signal integrity settings for each Tx and Rx lane, respectively.

If the ExplicitControl bit for a lane is set in the Data Path Configuration (see Table in section 3.3.4), the contents of the registers for that lane described below originate from corresponding registers in one of the Staged Control Sets.

If the ExplicitControl bit for a lane is cleared, the contents of the registers for that lane in the Table below were determined by the module according to the selected Application.

Indicators for Active Control Set, Rx Controls (Page 11h)

Address	Bits	Name	Description	Default Value	Type
Page11h 223	7-4	OutputEqPreCursorTargetRx2	**ACS::OutputEqPreCursorTargetRx<i>** Rx output pre-cursor equalization for lane <i> encoded as per Table in section 3.2.2 Advertisement: 01h:162.4-3	0x4	RO
	3-0	OutputEqPreCursorTargetRx1		0x4	RO
Page11h 224	7-4	OutputEqPreCursorTargetRx4		0x4	RO
	3-0	OutputEqPreCursorTargetRx3		0x4	RO
Page11h 225	7-4	OutputEqPreCursorTargetRx6		0x4	RO
	3-0	OutputEqPreCursorTargetRx5		0x4	RO
Page11h 226	7-4	OutputEqPreCursorTargetRx8		0x4	RO
	3-0	OutputEqPreCursorTargetRx7		0x4	RO
Page11h 227	7-4	OutputEqPostCursorTargetRx2	**ACS::OutputEqPostCursorTargetRx<i>** Rx output post-cursor equalization for lane <i> encoded as per Table in section 3.2.2 Advertisement: 01h:162.4-3	0x4	RO
	3-0	OutputEqPostCursorTargetRx1		0x4	RO
Page11h 228	7-4	OutputEqPostCursorTargetRx4		0x4	RO
	3-0	OutputEqPostCursorTargetRx3		0x4	RO
Page11h 229	7-4	OutputEqPostCursorTargetRx6		0x4	RO
	3-0	OutputEqPostCursorTargetRx5		0x4	RO
Page11h 230	7-4	OutputEqPostCursorTargetRx8		0x4	RO
	3-0	OutputEqPostCursorTargetRx7		0x4	RO
Page11h 231	7-4	OutputAmplitudeTargetRx2	ACS::OutputAmplitudeTargetRx<i> Rx output amplitude level for lane <i> encoded as per Table in section 3.2.2 Advertisement: 01h:162.2	0x2	RO
	3-0	OutputAmplitudeTargetRx1		0x2	RO
Page11h 232	7-4	OutputAmplitudeTargetRx4		0x2	RO
	3-0	OutputAmplitudeTargetRx3		0x2	RO
Page11h 233	7-4	OutputAmplitudeTargetRx6		0x2	RO
	3-0	OutputAmplitudeTargetRx5		0x2	RO
Page11h 234	7-4	OutputAmplitudeTargetRx8		0x2	RO
	3-0	OutputAmplitudeTargetRx7		0x2	RO

3.4.6 Data Path Conditions

After copying the settings for the lanes of a Data Path from a Staged Control Set to the Active Control Set during a successful Provision procedure triggered by ApplyDPInit (see Table 6-3 and Table 6-4 in section 6.2.4.2*), the module simultaneously sets the bits DPInitPendingLane<i> for the lanes <i> of that Data Path.
This indicates to the host that the Data Path configuration associated with Lane<i> has been updated (not necessarily modified) in the Active Control Set, whereas the subsequent transit through the DPInit state that will eventually commit the nominal settings in the Active Control Set to hardware is still pending.
When intervention-free reconfiguration is supported (by default, SteppedConfigOnly=0), these bits may also cause DPSM state transitions without further host intervention, as described in section 6.3.3.1*.

**Refer to CMIS 5.0*

Address	Bits	Name	Description	Default Value	Type
Page11h 235	0	DPInitPendingLane1	DPInitPendingLane<i> 0b: DPInit not pending 1b: DPInit not yet executed after successful ApplyDPInit, hence the Active Control Set content may deviate from the actual hardware configuration.	0	RO
	1	DPInitPendingLane2		0	RO
	2	DPInitPendingLane3		0	RO
	3	DPInitPendingLane4		0	RO
	4	DPInitPendingLane5		0	RO
	5	DPInitPendingLane6		0	RO
	6	DPInitPendingLane7		0	RO
	7	DPInitPendingLane8		0	RO

3.5 PRBS Generator

The Pattern Generator control is described in this section. The generated pattern is transmitted from the module to the host on the RX electrical output. The PRBS generator control registers are present in **Page 13h**. the PRBS generator mode is enabled automatically when the Loopback mode is disabled.

Address	Bit	Name	Description	Default Value	Type
144	7	HostSideGeneratorEnableLane8	0b: Disable pattern generator 1b: Enable pattern generator	0	RW (VR)
	6	HostSideGeneratorEnableLane7		0	
	5	HostSideGeneratorEnableLane6		0	
	4	HostSideGeneratorEnableLane5		0	
	3	HostSideGeneratorEnableLane4		0	
	2	HostSideGeneratorEnableLane3		0	

	1	HostSideGeneratorEnableLane2		0	
	0	HostSideGeneratorEnableLane1		0	
148	7-4	HostSideGeneratorPatternSelectLane2	The Pattern IDs are summarized below: 0: PRBS-31Q 1: PRBS-31 2: PRBS-23Q 3: PRBS-23 4: PRBS-15Q 5: PRBS-15 6: PRBS-13Q 7: PRBS-13 8: PRBS-9Q 9: PRBS-9 10: PRBS-7Q 11: PRBS-7 12: SSPRQ 13: Reserved 14: Custom 15: User Pattern	0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane1		0x0	
149	7-4	HostSideGeneratorPatternSelectLane4		0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane3		0x0	
150	7-4	HostSideGeneratorPatternSelectLane6		0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane5		0x0	
151	7-4	HostSideGeneratorPatternSelectLane8		0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane7		0x0	
176	7-4	HostPRBSGeneratorClockSource	0: All lanes uses Internal Clock 1: All lanes uses Recovered Clock Media Lane 1 2: All lanes uses Recovered Clock Media Lane 2 3: All lanes uses Recovered Clock Media Lane 3 4: All lanes uses Recovered Clock Media Lane 4 5: All lanes uses Recovered Clock Media Lane 5 6: All lanes uses Recovered Clock Media Lane 6 7: All lanes uses Recovered Clock Media Lane 7 8: All lanes uses Recovered Clock Media Lane 8 Ah-Eh: Reserved Fh: Recovered clock from Respective Media Lane/Datapaths are used	0b0000	RO (VR)
224-239	7-0	UserPattern	Host defined user pattern (16 Bytes)	-First 8 bytes: 0xFF -Last 8 bytes: 0x00	RW (VR)

3.6 PRBS Checker

The pattern Checker control is described in this section. The control is applied on the host side of the module for data received at the TX electrical input. The PRBS checker control registers are present in **Page 13h**. the PRBS checker mode is enabled by default.

The PRBS checker behavior described in this section is for the un-gated mode (13h:177.3-1 = 000b). In this mode, the error metrics measurement runs continuously. When the host enables the disabled PRBS checkers (register 160 in the table below) all error counters for the enabled

lanes are cleared and then start accumulating. When the host disables enabled PRBS checkers (register 160 in the table below) error counting is stopped, and error counting results will be available via Selector 01-05h.

The error information availability is related to the PeriodicUpdatesSupported settings (13h:129.4):

- 13h:129.4 = 0: real time error information is not updated and error information is only available when the error counting is stopped by checker disable
- 13h:129.4 = 1: real time error information is available with Selectors 01-05h. Update period is configured by 13h:177.0, as described in section 3.5.1.

The error counters and restart accumulation are controlled form ResetErrorInformation control bit 13h:177.5, as described in section 3.5.1.

Address	Bit	Name	Description	Default Value	Type
160	7	HostSideCheckerEnableLane8	0b: Disable pattern Checker 1b: Enable pattern Checker	1	RW (VR)
	6	HostSideCheckerEnableLane7		1	
	5	HostSideCheckerEnableLan6		1	
	4	HostSideCheckerEnableLane5		1	
	3	HostSideCheckerEnableLane4		1	
	2	HostSideCheckerEnableLane3		1	
	1	HostSideCheckerEnableLane2		1	
	0	HostSideCheckerEnableLane1		1	
164	7-4	HostSideCheckerPatternSelectLane2	The Pattern IDs are summarized below: 0: PRBS-31Q 1: PRBS-31 2: PRBS-23Q 3: PRBS-23 4: PRBS-15Q 5: PRBS-15 6: PRBS-13Q 7: PRBS-13 8: PRBS-9Q 9: PRBS-9 10: PRBS-7Q 11: PRBS-7 12: SSPRQ 13: Reserved 14: Custom 15: User Pattern	0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane1		0x0	
165	7-4	HostSideCheckerPatternSelectLane4		0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane3		0x0	
166	7-4	HostSideCheckerPatternSelectLane6		0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane5		0x0	
167	7-4	HostSideCheckerPatternSelectLane8		0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane7		0x0	
178	3-2	HostPRBSCheckerClockSource	0: Recovered clocks from Respective Host Lane/Datapaths are used	0b01	RO

			1: All lanes use Internal Clock 2: All lanes use reference clock 3: reserved		(VR)

3.6.1 PRBS Checker Lock Status

In PRBS Checker mode, the loss of lock (LOL) status is reported in register 138 of **Page 14h**.

Address	size	Name	Description	Default Value	Type
138	7	PatternCheckerLOLFlagHostLane8	-0b: no LOL is detected (Locked) -1b: LOL is detected (not Locked)	0	RO
	6	PatternCheckerLOLFlagHostLane7		0	
	5	PatternCheckerLOLFlagHostLane6		0	
	4	PatternCheckerLOLFlagHostLane5		0	
	3	PatternCheckerLOLFlagHostLane4		0	
	2	PatternCheckerLOLFlagHostLane3		0	
	1	PatternCheckerLOLFlagHostLane2		0	
	0	PatternCheckerLOLFlagHostLane1		0	

3.7 Loopback

The Host side loopback control registers are described in the table below. These registers are present in **Page 13h**. The Loopback mode is the default mode of the module. Writing 0x00 to register 183 will enable the PRBS Generator mode.

Address	size	Name	Description	Default Value	Type
183	7	HostSideInputLoopbackEnableLane8	-0b: PRBS Generator / Checker mode -1b: Retimed Loopback Mode Writing 1 to any of the register 183 bits will enable the Loopback mode on all channels.	1	RW (VR)
	6	HostSideInputLoopbackEnableLane7		1	
	5	HostSideInputLoopbackEnableLane6		1	
	4	HostSideInputLoopbackEnableLane5		1	
	3	HostSideInputLoopbackEnableLane4		1	
	2	HostSideInputLoopbackEnableLane3		1	
	1	HostSideInputLoopbackEnableLane2		1	
	0	HostSideInputLoopbackEnableLane1		1	

3.8 BER/SNR

The BER and SNR data and control are described in this section.

3.8.1 Error Information Reset and Update Period

The error information reset and update period control register 177 is present in Page 13h.

Address	Bit	Name	Description	Default	Type

				Value	
177	5	ResetErrorInformation	This bit is used to clear the error counters and restart accumulation of errors. -13h:177.5 = 1b: Currently accumulating error statistics identified by DiagnosticsSelector 01h to 05h are frozen -13h:177.5 = 0b: Error statistics identified by Selectors 01h-05h are reset to 0 When configuration in 13h:129.3=0b there is only 1 timer for all lane and all banks. Setting this bit to 1b: single gate timer is stopped Setting this bit to 0b: starts the single gating timer	0	RW (VR)
	0	UpdatePeriodSelect	Time between incremental updates to intermediate error counting results during a longer gating period 0b: 1 sec update interval 1b: 5 sec update interval	1	RW (VR)

3.8.2 Diagnostics Selector

The diagnostics selector is described in the table below. It is controlled from register 128 of **Page 14h**. This register controls the content of diagnostics data registers.

Address	Bit	Name	Description	Default Value	Type
128	7-0	DiagnosticsSelector	Select content of Diagnostics Data in bytes 192-255: -0x02: Host Lane 1-4 errors and total Bits counters (gives the host the ability to read the running BER while gating is in progress) -0x03: Host Lane 5-8 errors and total Bits counters (gives the host the ability to read the running BER while gating is in progress) -0x06: Host/Media Input Lane 1-8 SNR	0	RW (VR)

3.8.3 BER Diagnostics

The tables below show the registers reporting the errors count and the total bit counters for each channel. The mentioned registers are present in **Page 14h**. The reported channels are related to the value set in register 128 of page 14h as detailed in section 3.5.2.

For detailed info on how error count is reported, refer to section 3.3.

In case of 14h:128 = 0x02, check the table below.

Address	size	Name	Description	Default Value	Type

192-199	8	HostSideErrorCountLane1	U64 Little-endian error count Lane 1	0	RO (VR)
200-207	8	HostTotalBitsCountLane1	U64 Little-endian total bit count 1	0	
208-215	8	HostSideErrorCountLane2	U64 Little-endian error count Lane 2	0	
216-223	8	HostTotalBitsCountLane2	U64 Little-endian total bit count 2	0	
224-231	8	HostSideErrorCountLane3	U64 Little-endian error count Lane 3	0	
232-239	8	HostTotalBitsCountLane3	U64 Little-endian total bit count 3	0	
240-247	8	HostSideErrorCountLane4	U64 Little-endian error count Lane 4	0	
248-255	8	HostTotalBitsCountLane4	U64 Little-endian total bit count 4	0	

In case of 14h:128 = 0x03, check the table below.

Address	size	Name	Description	Default Value	Type
192-199	8	HostSideErrorCountLane5	U64 Little-endian error count Lane 5	0	RO (VR)
200-207	8	HostTotalBitsCountLane5	U64 Little-endian total bit count 5	0	
208-215	8	HostSideErrorCountLane6	U64 Little-endian error count Lane 6	0	
216-223	8	HostTotalBitsCountLane6	U64 Little-endian total bit count 6	0	
224-231	8	HostSideErrorCountLane7	U64 Little-endian error count Lane 7	0	
232-239	8	HostTotalBitsCountLane7	U64 Little-endian total bit count 7	0	
240-247	8	HostSideErrorCountLane8	U64 Little-endian error count Lane 8	0	
248-255	8	HostTotalBitsCountLane8	U64 Little-endian total bit count 8	0	

3.8.4 SNR diagnostics

The table below shows the registers reporting the SNR for each channel at the host side. The mentioned registers are present in **Page 14h**. In this case 14h:128 should be set to 0x06, as described in section 3.5.2.

Address	size	Name	Description	Default Value	Type
208-209	2	HostSideSNRLane1	U16 Little-endian in units of 1/256dB host lane 1 real time SNR	0	RO (VR)
210-211	2	HostSideSNRLane2	U16 Little-endian in units of 1/256dB host lane 2 real time SNR	0	
212-213	2	HostSideSNRLane3	U16 Little-endian in units of 1/256dB host lane 3 real time SNR	0	
214-215	2	HostSideSNRLane4	U16 Little-endian in units of 1/256dB host lane 4 real time SNR	0	
216-217	2	HostSideSNRLane5	U16 Little-endian in units of 1/256dB host lane 5 real time SNR	0	
218-219	2	HostSideSNRLane6	U16 Little-endian in units of 1/256dB host lane 6 real time SNR	0	

220-221	2	HostSideSNRLane7	U16 Little-endian in units of 1/256dB host lane 7 real time SNR	0	
222-223	2	HostSideSNRLane8	U16 Little-endian in units of 1/256dB host lane 8 real time SNR	0	

3.9 TX and RX Control Fields

This section lists the specific controls for each TX and RX lane. The control registers mentioned in this section are present in **Page 10h**.

Address	size	Name	Description	Default Value	Type
129	7	InputPolarityFlipTx8	Input Polarity Flip control: -0b: No TX input polarity flip -1b: Tx input polarity flip	0	RW (VR)
	6	InputPolarityFlipTx7		0	
	5	InputPolarityFlipTx6		0	
	4	InputPolarityFlipTx5		0	
	3	InputPolarityFlipTx4		0	
	2	InputPolarityFlipTx3		0	
	1	InputPolarityFlipTx2		0	
	0	InputPolarityFlipTx1		0	
137	7	OutputPolarityFlipRx8	Output Polarity Flip control: -0b: No RX Output polarity flip -1b: RX Output polarity flip	0	RW (VR)
	6	OutputPolarityFlipRx7		0	
	5	OutputPolarityFlipRx6		0	
	4	OutputPolarityFlipRx5		0	
	3	OutputPolarityFlipRx4		0	
	2	OutputPolarityFlipRx3		0	
	1	OutputPolarityFlipRx2		0	
	0	OutputPolarityFlipRx1		0	
138	7	OutputDisableRx8	Output Disable control: -0b: RX Output enabled -1b: RX Output disabled	0	RW (VR)
	6	OutputDisableRx7		0	
	5	OutputDisableRx6		0	
	4	OutputDisableRx5		0	
	3	OutputDisableRx4		0	
	2	OutputDisableRx3		0	
	1	OutputDisableRx2		0	
	0	OutputDisableRx1		0	

3.10 Advanced Configuration

The high-speed interface configuration such as taps, gray mapping, signal type and baud rate can be controlled from **Page B8h**. After any parameter is changed, apply configuration should be performed for the new settings take effect which can be done from register 130 of **Page B8h**.

Address	bit	Name	Description	Default Value	Type

128	2	Taps control	0: 3-Taps FIR Mode 1: 7-Taps FIR Mode	1	RW (NVR)
	1	Gray mapping	0: Gray mapping disabled 1: Gray mapping enabled	1	
	0	Signal type	0: PAM signal type 1: NRZ signal type	0	
129	7-0	Baud Rate Select	0: 25.78125 GBaud 1: 26.5625 GBaud 2: 41.25 GBaud 3: 51.5625 GBaud 4: 53.125 GBaud 5: 56.25 GBaud 6: 55.90474 GBaud* 7: 56.152354 GBaud* 8: 28.076177 GBaud*	4	
130	0	Apply Configuration	0 : do not apply 1 : Apply settings (self-clearing bit)	0	RW
131	0	Configuration mode	0: CMIS controls the high speed interface thorugh DataPath state machine, and controls the RXOUT EQ 1: User EEPROM pages B0 to B8 controls the above	0	RW (NVR)

Note: DSP configuration and RXOUT equalization are by default controlled from the CMIS registers in **Page 10h**.

If the user wants to use the advanced configuration, register 131 of **Page B8h** must be set to 1. This is an NVM register and only needs to be set once for switching between CMIS and advanced mode.

*: These rates are supported in HW RevD2 starting from FW 1.0 and HW RevD1 starting from FW 1.8.

3.11 Advanced Channel Configuration

RX output channels can be configured separately to tune the RX output signals. Each channel is controlled from a separate page, from B0h to B7h, for the register address range from 128 to 146.

The table below shows the page number corresponding to each channel.

Page Address	Description
B0	RXOUT 1 control page
B1	RXOUT 2 control page
B2	RXOUT 3 control page
B3	RXOUT 4 control page
B4	RXOUT 5 control page

B5	RXOUT 6 control page
B6	RXOUT 7 control page
B7	RXOUT 8 control page

After the page is the set, the corresponding parameters can be controlled, as described in the table below. Any change of the value in one of the following registers needs to apply configuration by writing 1 to register 130 **Page B8h**, as described in section 3.9.

Address	size	Name	Description	Default Value	Type
128	1	FIR Tap1 (MSB)	16-bit signed value: -1000 to +1000	0xFF	RW (NVR)
129	1	FIR Tap1 (LSB)		0xEE	
130	1	FIR Tap2 (MSB)	16-bit signed value: -1000 to +1000	0x00	
131	1	FIR Tap2 (LSB)		0x3A	
132	1	FIR Tap3 (MSB)	16-bit signed value: -1000 to +1000	0xFF	
133	1	FIR Tap3 (LSB)		0x5C	
134	1	FIR Tap4 (MSB)	16-bit signed value: -1000 to +1000	0x02	
135	1	FIR Tap4 (LSB)		0x2C	
136	1	FIR Tap5 (MSB)	16-bit signed value: -1000 to +1000	0xFF	
137	1	FIR Tap5 (LSB)		0x83	
138	1	FIR Tap6 (MSB)	16-bit signed value: -1000 to +1000	0x00	
139	1	FIR Tap6 (LSB)		0x27	
140	1	FIR Tap7 (MSB)	16-bit signed value: -1000 to +1000	0xFF	
141	1	FIR Tap7 (LSB)		0xD7	
142	1	PAM4 Lower Inner EYE (MSB)	16-bit unsigned value: 500 to 1500	0x03	
143	1	PAM4 Lower Inner EYE (LSB)		0xE8	
144	1	PAM4 Upper Inner EYE (MSB)	16-bit unsigned value: 1500 to 2500	0x07	
145	1	PAM4 Upper Inner EYE (LSB)		0xD0	
146	1	Swing adjustment	Control the amplitude adjustment: -60% : 0x3C -70%: 0x46 - 80%: 0x50 - 90%: 0x5A -100%: 0x64 -110% : 0x6E -120%: 0x78	0x46	

4 Module Connectivity

The **ML4062-ALB1-2A/B-112** has a front USB-C connector allowing the user to access the following features:

- Reload registers
- FW upgrade

5 QSFP-DD Pin Allocation

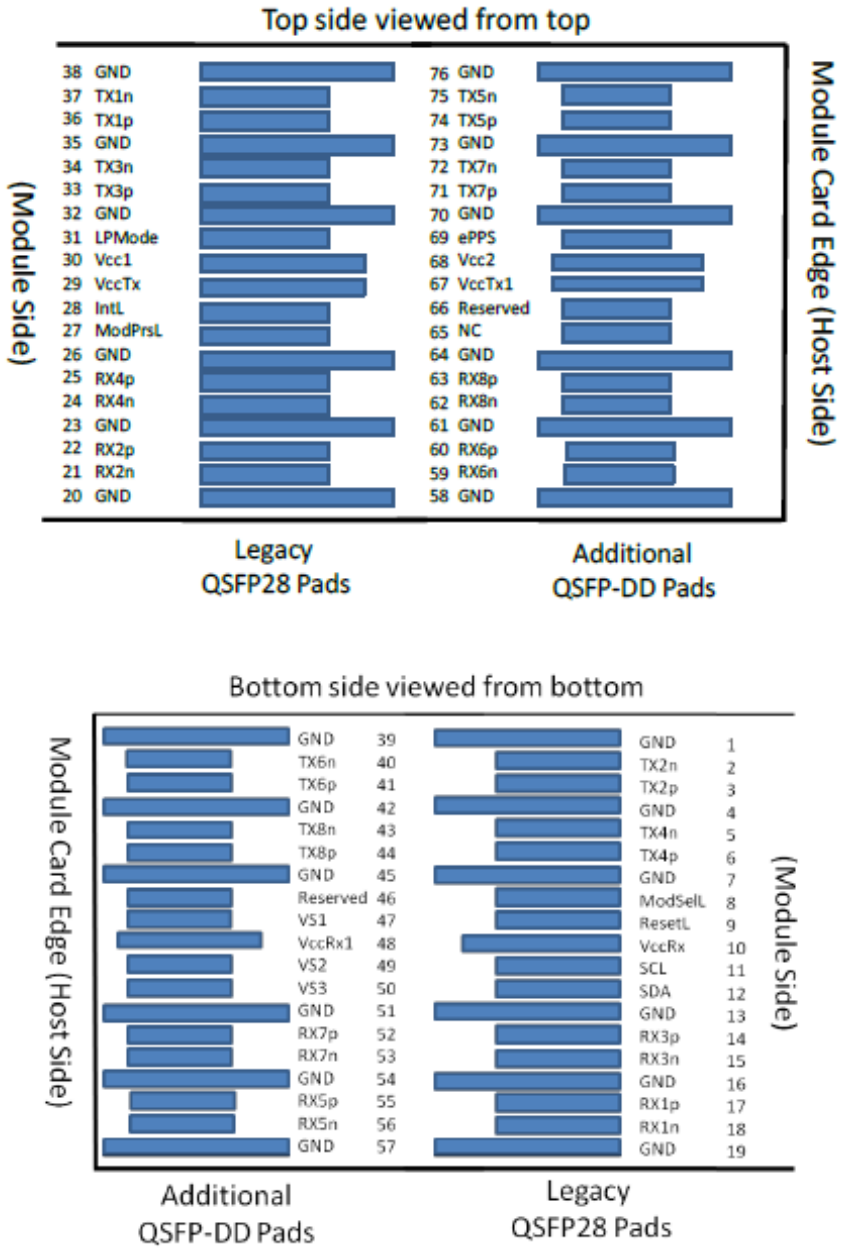

Figure 8: QSFP-DD Module Pad Layout

6 Mechanical Dimensions – ML4062-ALB1-2A-112

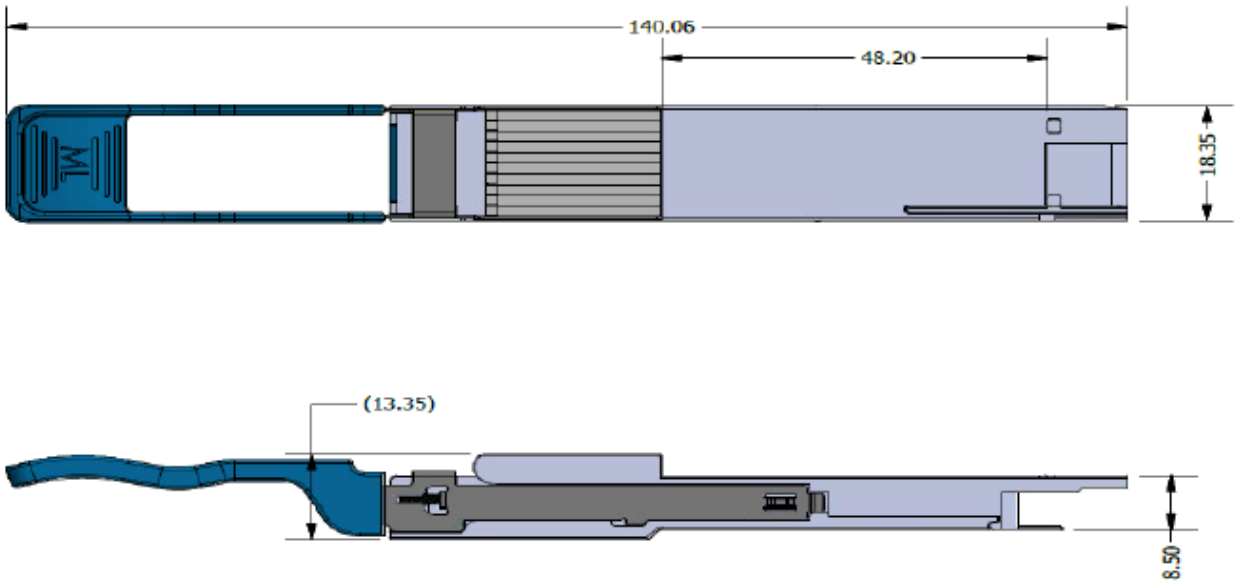

Figure 9: Mechanical Dimensions

7 Major FW Upgrades

Firmware upgrades are summarized in this section.

Latest FW release is **V1.7**.

FW Release	Upgrades
V1.1	▪ Initial FW release
V1.2	▪ Line-Side lane count interface changed to 8 instead of 0. ▪ AppSel code 2 memory location space is moved between address 90 and 93 of low memory page.
V1.3	▪ Supported Signal Integrity Controls Advertisement register 161 bit 3 of PAGE01 is changed to 1 to indicate Adaptive TX input EQ support.
V1.4	▪ Media Lane Assignment Advertising registers 176 and 177 of PAGE01 values are changed to 0x01. Application is allowed to begin on Media Lane 1 for AppSel 1 and AppSel 2.
V1.5	▪ PAGE 11h is added to support active control set, Data Path state machine status and data path lane configuration status ▪ Added 2 additional AppSel codes 3 and 4 for 1x400G (8x26.5625GBaud PAM4) and 1x200G (8x26.5625GBaud NRZ) ▪ Added Datapath and RXOUT EQ control through Apply trigger registers ApplyImmediate and ApplyDataPathInit ▪ Added implementation of explicit control in both direction (from host or from module) ▪ Added 4 levels amplitude CMIS registers control ▪ Added 8 levels PRE/Post-cursor CMIS register control ▪ Added advertisement registers and support registers for the above ▪ Added revert back event for returning the pre/post/main taps to factory settings using the User EEPROM register space (old configuration not CMIS) ▪ previous configuration through User EEPROM address space is still available but by default it is OFF, when setting register 131 of PAGEB8 to 1, user will be able to set the DSP and lane configuration through user EEPROM registers in pages B0 to B8

V1.6	▪ Added 4 additional AppSel codes : 5 (8x53.125 PAM4), 6 (4x53.125 PAM4), 7 (1x26.5625G PAM4), and 8 (1x25.78125G NRZ) ▪ Added RX EQ setting for long channel appsel codes 5 and 6 to support channel up to 12-14dB ▪ Advertisement for DPDeinit and DPinit max state duration is set to correct duration ▪ De-initializing any Data Path host lane though registers address 128 of Page 10h will not change the module state, only Data Path state machine will continue to operate normally.
V1.7	▪ Added 3 additional AppSel codes : 9 (1x53.125 PAM4), 10 (1x53.125 PAM4), 11 (4x25.78125 NRZ) ▪ Added DSP validation after chip mode update or change. Validation results are loaded in Page03 (user EEPROM) for internal debugging. ▪ Updated advertisement register values for AppSel codes 2, 6, 7, and 8. ▪ Updated channel numbering of initial AppSel code loaded on Active and Control. It will always start on channel 0. ▪ Updated Supported Controls Advertisement Media side to remove support of TXOUT disable control. ▪ Updated Supported Controls Advertisement Host side to include support of RXOUT disable control and polarity inversion. ▪ Reading Lock and BER registers from DSP is now prohibited when module is in DPDeinit state. ▪ MCU GPIO direction for LPMode pin is changed to input to allow proper reading of the LPMode signal.
V1.8	▪ Added 3 custom baudrate : 55.904735GBaud PAM4 and NRZ ,56.152354GBaud PAM4 and NRZ 28.076177GBaud PAM4 and NRZ. ▪ Module Init time or Max Time to reach manageability in ModuleLowPwr as per CMIS 5.0 is reduced to 1600us, the timing is now compliant to CMIS 5.0 specs . ▪ Max duration module power up advertisement register value is fixed to indicate correct time between 1 and 5s.

Revision History

Revision number	Date	Description
0.1	8/10/2021	▪ Preliminary
0.2	9/6/2021	▪ Preliminary ▪ Update PN ▪ Update CMIS version to 5.0 ▪ Add Ordering Information section
0.3	10/5/2021	▪ Preliminary ▪ Add section 3 ▪ Add section 4
0.4	10/6/2021	▪ Preliminary ▪ Update section 3.3 ▪ Fix typos in section 3
0.5	11/8/2021	▪ Preliminary ▪ Update EEPROM content table ▪ Update register addresses sections 2.4.4, 2.4.11, 2.4.12 and 2.4.13 ▪ Update default values in tables sections 3.2 and 3.3 ▪ Update byte size section 3.5.4
0.6	11/11/2021	▪ Preliminary ▪ Update section 3 ▪ Update section 3.2 ▪ Update section 3.4 ▪ Update section 3.5.1 ▪ Add section 3.3.1 ▪ Add section 3.7 ▪ Add section 3.8
0.7	12/22/2021	▪ Preliminary ▪ Fix the Page number in sections 3.5.3 and 3.5.4
0.8	9/15/2022	▪ Update section 2.2.3 ▪ Update section 2.2.4 ▪ Update section 2.4.4 ▪ Update section 2.4.6 ▪ Update section 3.2 ▪ Update section 3.3 ▪ Update section 3.8
0.9	10/1/2022	▪ Update section 2.2.3 ▪ Add section 3.1.1 ▪ Update section 7
1.0	10/28/2022	▪ Update section 2.2.3 ▪ Update section 3.1.1 ▪ Update section 7

1.1	12/20/2022	▪ Update section 2.1.4 ▪ Update section 2.2.3 ▪ Fix section 2.4.4 ▪ Update section 3.1.1 ▪ Add section 3.2 and 3.3 ▪ Update section 7
1.2	12/23/2022	▪ Update section 2.2.3 ▪ Update section 3.1.1 ▪ Update section 3.2.1 ▪ Update section 3.9 ▪ Update section 7
1.3	1/26/2023	▪ Update section 2.2.3 ▪ Update section 3.1.1 ▪ Update section 3.2.1 ▪ Update section 7
1.4	6/20/2023	▪ Added Section 3.1 Supported Rates
1.5	3/28/2024	▪ Update section 3.10 ▪ Update section 7

North America
48521 Warm Springs Blvd. Suite 310
Fremont, CA 94539
USA
+1 510 573 6388

Worldwide
Houmal Technology Park
Askarieh Main Road
Houmal, Lebanon
+961 81 794 455

Asia
14F-5/ Rm.5, 14F., No 295
Sec.2, Guangfu Rd. East Dist.,
Hsinchu City 300, Taiwan (R.O.C)
+886 3 5744 591